Study Of Low Frequency Noise And Electronic Transport In 2D Van-der Waals Material And Their Functional Devices

A thesis

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By

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To

Maa & Baba

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Abstract

The physics of two-dimensional materials has attracted attention since the isolation of a single sheet of graphene in 2004. Following the discovery a plethora of van der Waal materials can be found in different forms such as ferromagnets (CrI_3), semiconductors (MoS_2, BP), insulator (hBN), superconductors ($NbSe_2$), and even with exotic topological properties (WTe_2, twisted bilayer graphene). By mixing and aligning these 2D materials on top of each other or by functionalizing them with nanoparticles, improved functionalities can be incorporated into these 2D materials. Due to their distinctive surface character, 2D materials experience both intrinsic and extrinsic disorders significantly affecting their transport characteristics. The importance of intrinsic and extrinsic disorder in charge transport, as well as proximity-induced functionalization of these 2D materials, are the primary topics of this thesis. To explore these characteristics, we have focused on the electrical transport and low frequency noise measurements as a function of temperature and gate voltage by fabricating micron-scale field effect devices from these 2D materials. In particular, noise data being more sensitive compared to the time averaged conductivity, provides insight about the mobile scattering mechanisms due to the mobile defects involved in the electrical transport.

In the first half of the thesis, we have performed a detail investigation of electrical transport and low frequency 1/f noise measurement to understand the role defects of lightly doped Si/SiO_2 substrate on the transport properties of graphene field effect transistor (FET). We have shown that the conductance fluctuations in the graphene channel is enhanced significantly near the depletion region which is 300 nm far away from the graphene channel, describing the sensitivity of noise to the remote charge fluctuations inside the depletion region. We next focused on functionalizing graphene using organometallic spin crossover (SCO) nanoparticle, which can change its spin state by the application of external stimuli like pressure or temperature. We could successfully create CVD graphene-SCO hybrid devices, exhibiting tunable hysteresis with varying gate voltages. More interesting behavior was observed in rGO/SCO hybrid. While the hysteresis width and transition temperature can be controlled via molecular concentration variation, magnetic measurements reveals improved cooperativity from interfacial charge transfer-induced intermolecular interactions. In the second half, we present electrical transport and noise study on FET fabricated from few layer thick Tellurene (Te), a narrow gap 2D semiconductor, synthesized using hydrothermal method. The hydrothermally grown Te devices shows high mobility with a

dominant p-type character, however, could show ambipolar character by choosing suitable contact metal. A metal-to-insulator transition was observed in these devices, occurring at high carrier densities, is dependent on the mobility of the device as revealed by temperature-dependent transport studies. Noise measurements indicate a typical 1/f type behavior across the entire range of gate voltages, originating primarily due to the mobility fluctuations arising from carrier scattering by the lattice. Thus, our study sheds light not only on the substrate induced transport characteristics in these 2D devices, but also demonstrate an interesting insight in SCO/2D hybrid.

List of publications

Publications included in the thesis

1. "Sensing remote bulk defects through resistance noise in a large area graphene field effect transistor**"**
   Shubhadip Moulick, Rafiqul Alam and Atindra Nath Pal
   ACS Appl. Mater. Interfaces 2022, 14, 45, 51105–51112

2. "Electronic transport and low frequency noise in elemental 2D Tellurene field effect transistors**.**"
   Shubhadip Moulick, Dipanjan Maity, Kalyan Mandal and Atindra Nath Pal
   (Manuscript ready to be submitted**)**

3. "Tuning cooperativity and magnetic coupling in spin-croosover-2D hybrid heterostrctures via interfacial charge transfer interaction "
   Shatabda Bhattacharya, **Shubhadip Moulick**, Chinmoy Das, Shiladitya Karmakar, Hirokazu Tada, Tanushri Saha Dasgupta, Tatsuhiko Ohto, Shinji Kitao, Makoto Seto, Pradip Chakraborty and Atindra Nath Pal
   (Manuscript under review**)**

Other Publication not covered in the thesis

1. "G Phonon Mode Splitting in Doped Bilayer Graphene Probed by in-situ Transport Measurement and Raman Spectroscopy"
   Shubhadip Moulick, Shubhrasish Mukherjee, Shreyan Raha, Achintya Singha and Atindra Nath Pal
   AIP conference proceeding 2022.

2. "Flicker noise in an electrolyte gated large area Gr-FET"
   Rafiqul Alam, **Shubhadip Moulick**, Atindra Nath Pal
   AIP conference proceeding 2022.

3. "Valley polarization and photocurrent generation in transition metal dichalcogenide alloy $MoS_{2x}Se_{2(1-x)}$"

   Chumki Nayak, Suvadip Masanta, Sukanya Ghosh, **Shubhadip Moulick**, Atindra Nath Pal and Achintya Singhya

   (Accepted in PRB)

4. " Tuning of magnetic frustration and emergence of a magnetostructural transition in $Mn_{1-x}Cd_xCr_2O_4$"

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Commonly Used Abbreviation

AFM	Atomic force microscope
BLG	Bilayer graphene
hBN	Hexagonal Boron Nitride
TMDC	Transition Metal Dichalcogenide
CNP	Charge neutrality point
CVD	Chemical vapor deposition
DOS	Density of states
DFT	Density Functional Theory
CBM	Conduction band minima
VBM	Valance band maxima
DP	Dirac point
FLG	Fewlayer graphene
GraFET	Graphene field effect transistor
HOPG	Highly Oriented Pyrolytic Graphite
IPA	Isopropyl alcohol
MLG	Multilayer graphene
MOSFET	Metaloxidesemiconductor field-effect transistor
PMMA	Polymethyl methacrylate
PSD	Power spectral density
SEM	Scanning electron microscope
TEM	Transmission electron microscopy
SLG	Single layer graphene
UCF	Universal conductance fluctuations
VRH	Variable range hopping
BP	Black Phosphorus
rGO	Reduced graphene oxide
GO	Graphene oxide
SCO	Spin cross-over

Contents

Chapter 1

Introduction

In 2004, the isolation of a single layer of graphite, known as Graphene[1], sparked interest in the physics of 2D materials. Following the discovery of graphene, a plethora of materials with a wide range of physical properties were found, including semimetals (Graphene) [2,3], insulators (hBN) [4], semiconductors (MoS_2, WS_2, Te, BP) [5–11], ferromagnets (CrI_3, Fe_3GeT_2), superconductors ($NbSe_2$), and more. These van der Waals materials reveal fascinating characteristics when reduced to their monolayer or bilayer limits through the process of mechanical exfoliation. For instance, graphene, as a monolayer film, possesses a linear Dirac-like band dispersion, while the dispersion becomes parabolic for bilayer graphene[12]. Likewise, MoS_2 undergoes a transition from an indirect to a direct band gap semiconductor as its thickness decreases to a monolayer[5]. The exceptional properties of these 2D materials have established a new platform for next-generation electronic and opto-electronic devices[13]. Prototypes of circuit-level implementations of 2D FETs, such as inverters, logic operators, and radio-frequency devices, have already been achieved. While the initial prototypes relied on exfoliated flakes, the 2D community has swiftly transitioned towards growing large-area films using chemical vapor deposition (CVD) techniques[14–16]. Mixing and aligning these 2D materials on top of each other using dry transfer techniques provides an opportunity to study improved device functionalities, as well as leading to observations of interesting physical phenomena like the Hofstadter Butterfly[4], Valley Hall effect[17], Columb drag[18], superconductivity[19], and other correlated phases. Due to the large surface area of these 2D materials, new functionalities can be added by combining them with semiconducting nanoparticles[20], functional molecules[21], plasmonic nanoparticles[22], and so on, creating an opportunity to explore proximity-induced new functional devices.

This chapter briefly introduces about various 2D materials namely, Graphene and 2D semiconductors. We will discuss their electronic properties to understand the results of the various transport measurement in the subsequent chapters.

1.1 Graphene

1.1.1 Crystal structure

Graphene is composed of a single layer of carbon atoms arranged in a hexagonal lattice. In the atomic ground state, each carbon atom possesses six electrons distributed in the $1s^2 2s^2 2p^2$ configuration, with two electrons filling the inner 1s orbital and four electrons occupying the outer shell of 2s and 2p orbitals. The honeycomb lattice does not qualify as a Bravais lattice due to the lack of equivalence between neighboring sites. However, both the A and B sublattices constitute triangular Bravais lattices. Consequently, the honeycomb lattice can be regarded as a triangular Bravais lattice with a two-atom basis (A and B), as depicted in **Figure 1.1a**. The primitive lattice vector of graphene lattice is written as

$$\overrightarrow{a_1} = \frac{a}{2}(3, \sqrt{3}) \quad , \quad \overrightarrow{a_2} = \frac{a}{2}(3, -\sqrt{3}) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1.1)$$

Where $a = 1.42$ Å is the C-C distance. The reciprocal lattice of graphene is also hexagonal as shown in **Figure 1.1b**, and the reciprocal lattice vectors are given by

$$\overrightarrow{b_1} = \frac{2\pi}{3a}(1, \sqrt{3}) \quad , \quad \overrightarrow{b_2} = \frac{2\pi}{3a}(1, -\sqrt{3}) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1.2)$$

Γ, *M* and *K* are the high symmetry points in the Brillouin zone. The *K* and *K′* points, located at the corners of the Brillouin zone are of particular interest for the physics of graphene and they are called the Dirac points. Their co-ordinates are given by the vectors

$$\vec{K} = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right) \quad , \quad \vec{K}' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1.3)$$

The three nearest neighbor vectors in real space are given by

$$\overrightarrow{\delta_1} = \frac{a}{2}(1, \sqrt{3}) \quad , \quad \overrightarrow{\delta_2} = \frac{a}{2}(1, -\sqrt{3}) \quad , \quad \overrightarrow{\delta_3} = a(-1, 0) \ldots\ldots\ldots\ldots (1.4)$$

Graphene possesses identical sublattices due to its uniform arrangement of carbon atoms. This symmetry results in sublattice A transforming into sublattice B, and vice versa, under the space inversion operation (x → − x and y → − y). Consequently, graphene exhibits inversion symmetry. Additionally, single-layer graphene (SLG) maintains time reversal symmetry. The interplay of

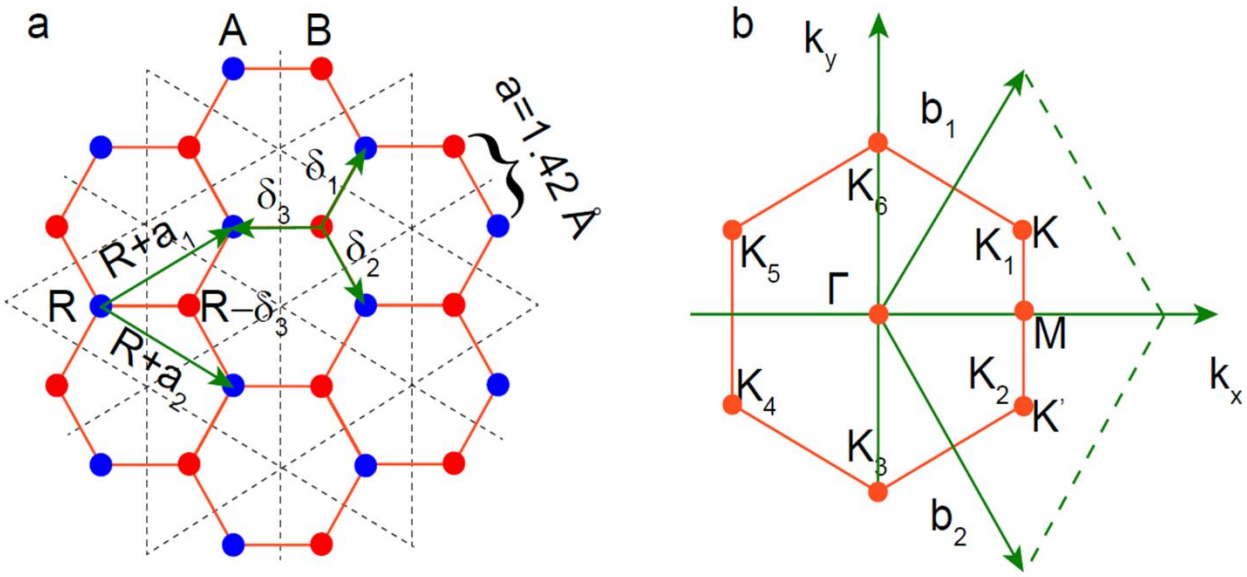


Figure 1.1. *(a) Schematic of the crystal structure of Graphene. The blue sites and red sites denote the A and B sublattice respectively. The two lattice vectors a_1, a_2 and three vectors joining the nearest neighbours 1, 2, 3 are also shown. The dashed grid shows the triangular Graphene lattice. The whole crystal can be constructed by shifting the unit cell with two basis atoms by the lattice vectors a_1 and a_2. (b) First Brillouin zone of Graphene. The reciprocal vectors are denoted by b_1 and b_2. The high symmetry points are marked. All the corners of the rest Brillouin zone are high symmetry points but only two successive points (K and K_0) are independent. Rest of the corner points can be attained translating those two points by the reciprocal vectors.*

these two symmetries renders SLG a zero band gap material. In contrast, hexagonal boron nitride (hBN) features sublattice A with boron atoms and sublattice B with nitrogen atoms. This uneven distribution disrupts the inversion symmetry, leading to the creation of a substantial band gap (approximately $5 - 6$ eV for hBN)[23]. This characteristic renders hBN an atomically smooth substrate and an effective gate dielectric for 2D materials.

1.1.2 Band structure of Graphene

The electronic band structure of graphene was determined using the tight-binding formulation. This method involved considering various hopping energies to analytically calculate the dispersion of electronic states. P.R. Wallace[24] pioneered this computational approach in 1947. It relied on the Hamiltonian for the tight-binding approximation, which accounts for interactions between atoms at the nearest and next-nearest positions. The Hamiltonian[2526], expressed as follows:

$$H = -t\sum_{<i,j>,\sigma}\left(a^{\dagger}_{\sigma,i}b_{\sigma,j} + H.C.\right) - t'\sum_{<i,j>,\sigma}\left(a^{\dagger}_{\sigma,i}a + b^{\dagger}_{\sigma,i}b_{\sigma,j} + H.C.\right) \quad \text{..... (1.5)}$$

where, $a^{\dagger}_{\sigma,i}$ and $a_{\sigma,i}$ are the creation and annihilation operators for an electron with spin σ ($\sigma = \uparrow\downarrow$) on the A sublattice at site R_i. Similarly, $b_{\sigma,i}$and $b^{\dagger}_{\sigma,i}$ pertain to the B sublattice. These summations encompass all neighboring atoms, and the Hermitian conjugate (H.C.) of the operator. The energy associated with nearest neighbor hopping between different sublattices is denoted as t (approximately 2.8 eV), while the next nearest neighbor interactions within the same sublattice are characterized by t' (approximately 0.1 eV). These parameters govern the electron dynamics in the Graphene lattice, influencing how electrons move and interact within the material. Solving the

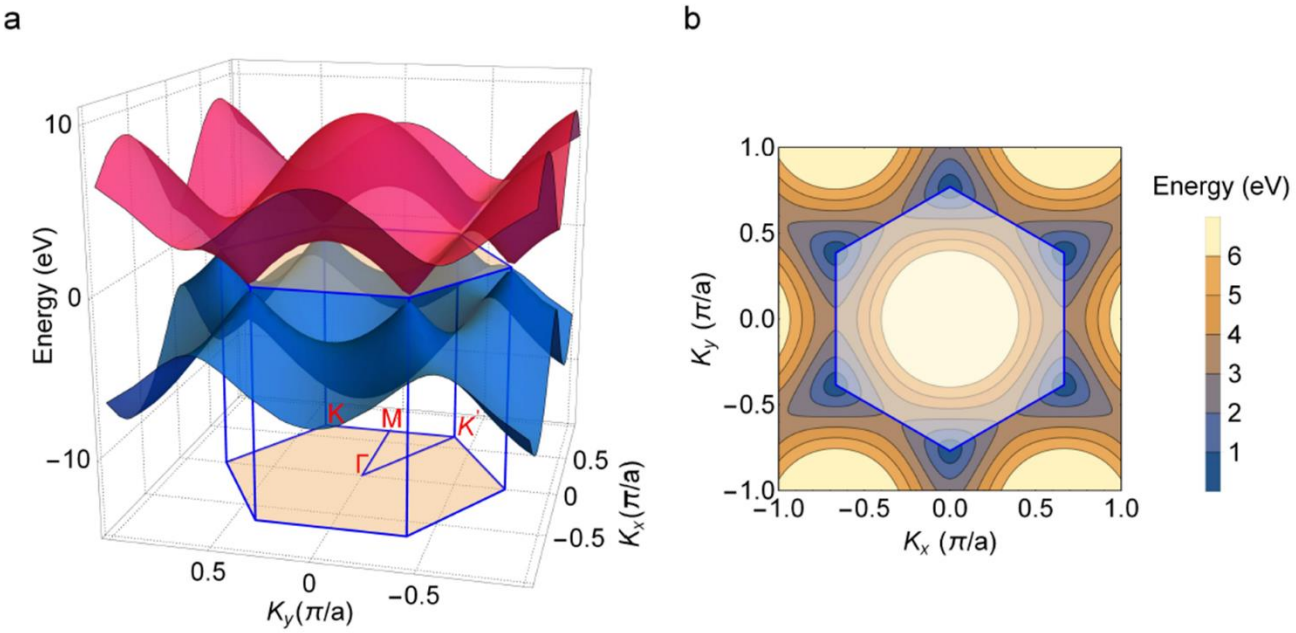


Figure 1.2. *(a) 3D plots of the conduction and the valence band. The first Brillouin zone is also marked by the blue hexagon. (b) Contour plot of the conduction band with the first Brillouin zone superimposed on it. It shows that the Fermi contours are trigonally warped at high energy.*

tight binding Hamiltonian one can get the dispersion relation in the form:

$$E_{\pm}(\vec{k}) = \pm t\sqrt{3 + f(\vec{k})} - t'(\vec{k}) \quad \text{.....(1.6)}$$

$$f(\vec{k}) = 2\cos(\sqrt{3}k_y a) + 4\cos\left(\frac{\sqrt{3}}{2}k_y a\right)\cos\left(\frac{3}{2}k_x a\right) \quad \text{.....(1.8)}$$

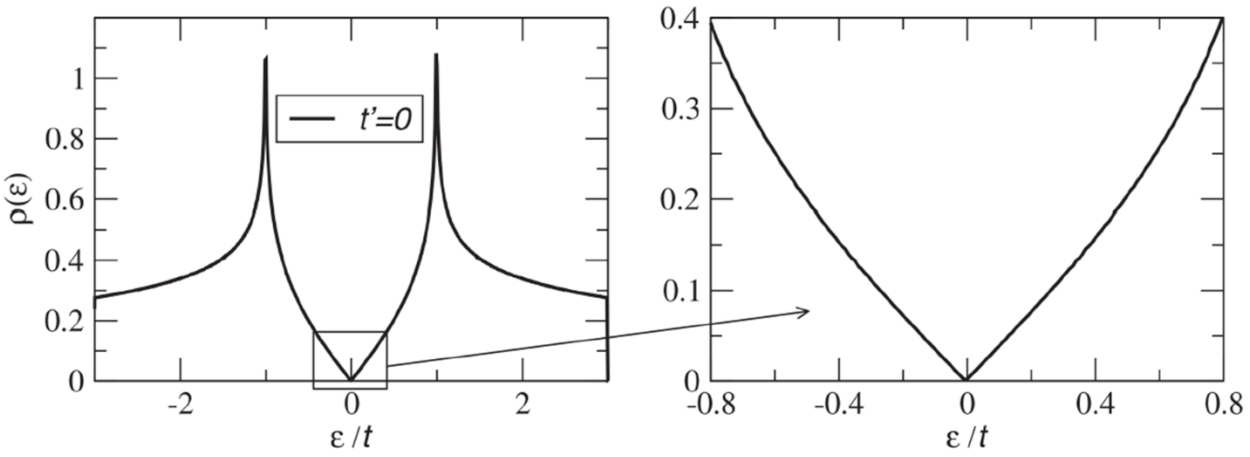


Figure 1.3. *Density of states (DOS) per unit cell as a function of energy. The zoomed-in version of the DOS is linear at lower energies. (Adopted from ref. [25])*

In Equation 1.6, the plus sign corresponds to the upper $\pi*$ (Conduction band) while the minus sign represents the lower π (valence band). Due to the significant difference in magnitude between the t' term and the t term, the contribution of t' can be safely disregarded. This simplification leads to a symmetric energy dispersion for electron-hole pairs, where the valence and conduction bands touch at six points within the Brillouin zone, as depicted in **Figure 1.2a**. These specific points, denoted as K and K′, are referred to as the Dirac points.

The complete band structure of graphene, as derived from Equation 1.8, is illustrated in **Figure 1.2a.** Additionally, a detailed view of the dispersion near one of the Dirac points at either K or K' is provided. Through an expansion of the full band structure, as described in Equation 1.8, in the vicinity of the K (or K') vectors expressed in Equation 1.3, specifically when $|q| << K$, we arrive at the following expression:

$$E_{\pm}(q) \approx \pm v_F|q| + \mathcal{O}[(q/K)^2] \quad \text{.....} \quad (1.9)$$

Here, q represents the momentum measured with respect to the Dirac points, and v_F denotes the Fermi velocity. The specific value of $v_F$is determined by v_F = 3ta/2ħ ≈ $1 \times 10^6\ m/s$. Notably, the remarkable characteristic of this low-energy dispersion relation is its linearity. This is in contrast to the parabolic energy dispersion typically observed in a general 2D structure, a distinction made particularly evident when we omit consideration of next-nearest neighbor hopping. The density of states is given by

$$\rho(E) = \frac{2A_C}{\pi}\frac{E}{|v_F|^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1.10)$$

Where $A_C = 3\sqrt{3}a^2/2$ is the unit cell area. Close to the Dirac point, the density of states varies linearly in energy. The Dirac point is also called a charge neutrality point (CNP) due to the vanishing DOS at $E_F = 0$. Below the CNP, the charge carriers are considered as hole type, and they are considered as electron type for $E_F > 0$.

1.1.3 Vibrational Properties of Graphene

The unit cell of single-layer graphene possesses two atom bases (A and B), with its atoms exhibiting both in-plane and out-of-plane motion, resulting in a total of three degrees of freedom (x, y, z). Consequently, there are six branches in total: three optical (LO, TO, and ZO) and three acoustic (LA, TA, and ZA). The phonon dispersion of single-layer graphene along high symmetry lines is depicted in **Figure 1.4a**, employing density functional theory (DFT). In the optical branches, LO represents in-plane longitudinal optic mode, TO signify in-plane transverse optic mode, and ZO corresponds to the optical mode in the perpendicular direction. Similarly, in the acoustic branches, LA denotes in-plane longitudinal acoustic mode, TA indicates in-plane transverse acoustic mode, and ZA represents the acoustic mode in the perpendicular direction. For the characterization of sp^2 and sp^3 carbon materials like graphite, diamond, poly-aromatic compounds, carbon nanotubes, and fullerenes, Raman spectroscopy proves effective as a non-

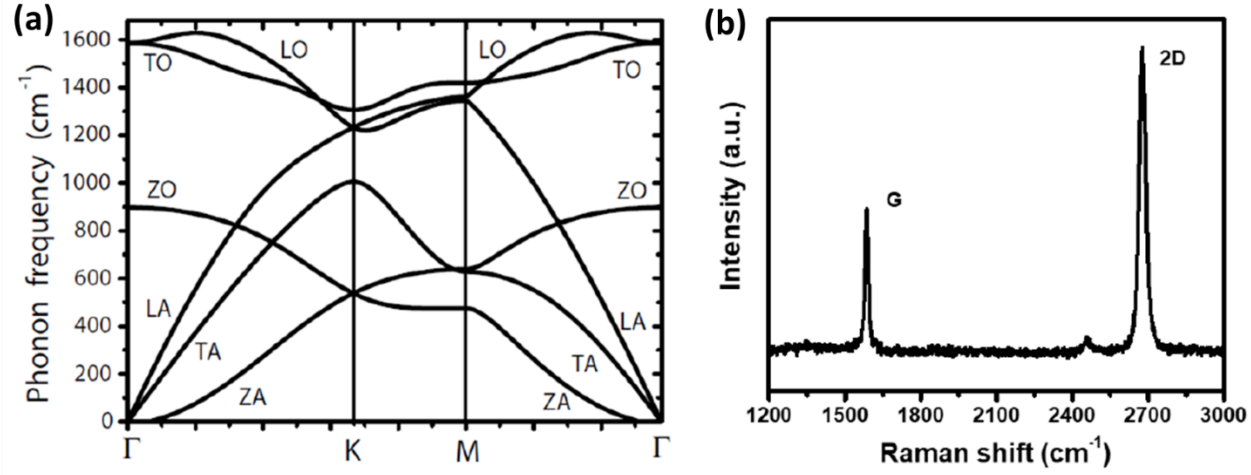


Figure 1.4. *(a) Phonon dispersion relation in single layer Graphene. (b) Raman spectra of a typical Graphene layer showing its characteristics G and 2D peak. (Adopted from ref. [12])*

invasive and non-destructive tool. It has been uniquely employed to determine the number of graphene layers, with Raman fingerprints differing between single and bilayer graphene[12]. **Figure**

1.4b illustrates a typical Raman spectrum of monolayer graphene with 532 nm laser excitation. The symmetry allows the E_{2g} mode at the Γ point, commonly known as the G mode, to appear at 1583 cm^{-1}. Irrespective of the number of layers, the G-band frequency remains constant. The most distinguishing feature of the Raman spectrum is the 2D-band, which varies based on the number of layers. The layer dependency (n = 1, 2, 3, 4, etc.) of the graphene 2D-band is represented in

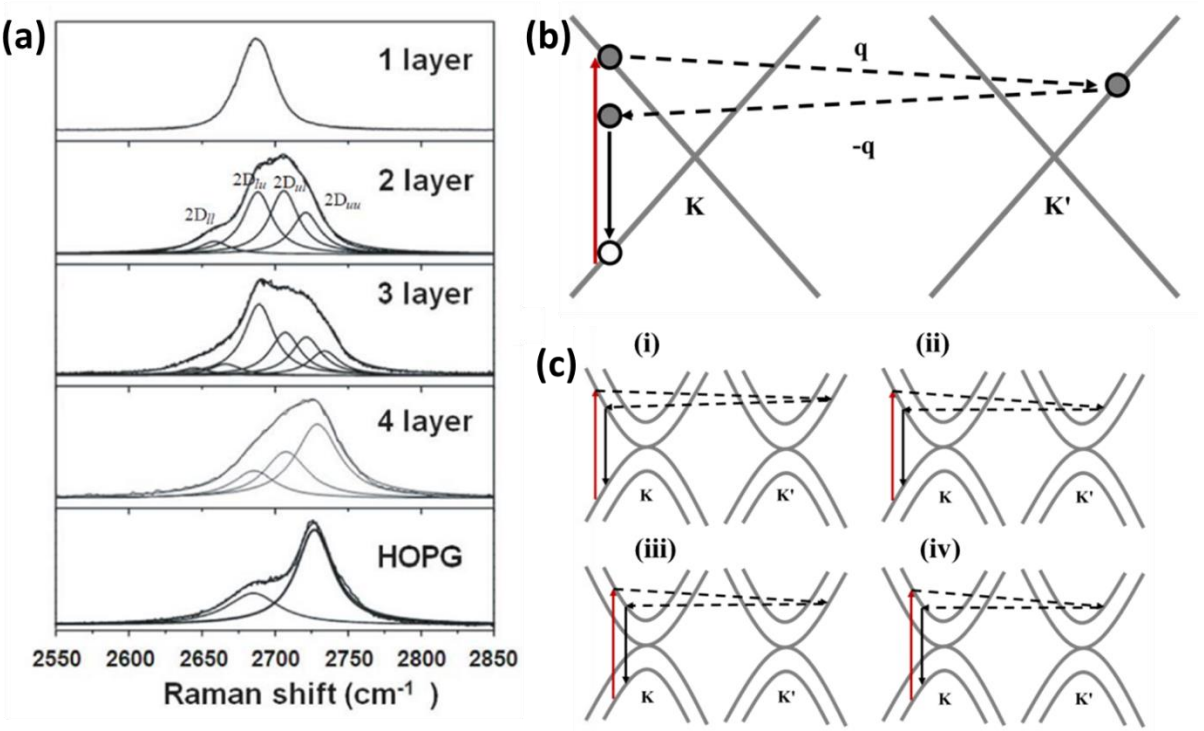


Figure 1.5. *(a) Layer dependent evolution of 2D peak in graphene, adapted from ref. [12]. (b) 2nd order Raman process in single layer graphene. (c) Origin of the 4 peaks for the bilayer graphene system*

Figure 1.5a. In single-layer graphene, the 2D-band is a single band with a Full Width at Half Maximum (FWHM) of approximately 25 cm^{-1} and a wavelength of 2685 cm^{-1}. In contrast, the 2D-band in bilayer graphene can be effectively deconvoluted into four Lorentzians, namely 2Duu, $2D_{ul}$, $2D_{lu}$, and $2D_{ll}$, as illustrated in **Figure 1.5c**. For 3 layers (n = 3), the 2D band is decomposed into six components, and beyond n>5, the 2D mode becomes indistinguishable from Highly Oriented Pyrolytic Graphite (HOPG), which can be bifurcated into two components. The Raman 2D-band lineshape's dependence on the number of layers is elucidated by the double resonance (DR) mechanism, incorporating the layer-dependent electronic band structure. The DR process for single-layer graphene is delineated in **Figure 1.5b**, accounting for the singular 2D-band. However, in bilayer graphene, inter-layer coupling induces a splitting of the conduction and valence bands

at the K and K' points, as depicted in **Figure 1.5c**. The four sub-bands observed in the 2D spectrum arise from four possible inter-valley transitions in the "e-h" process, involving the upper (u) and lower (l) bands. The stacking sequence can also be ascertained by examining the 2D-band. For instance, when comparing ABC-stacked tri-layer to ABA (Bernal stacking), the peaks exhibit a blue shift.

1.2 Two dimensional Semiconductors

1.2.1 Transition Metal Dichalcogenide (TMDC)

The bulk crystal of transition metal dichalcogenide (TMDC), akin to graphene, consists of monolayers connected by weak van der Waals forces. These TMDC monolayers are composed of transition metal atoms (M = Mo, W, Nb) sandwiched between two layers of chalcogen atoms (X = S, Se, Te), resulting in the MX_2 structure. Utilizing the exfoliation technique, the layers can be thinned down to monolayers from the original bulk crystal, facilitated by the feeble interaction between them. While most TMDCs exhibit semiconductor[5,27–33] properties (such as MoS_2, WSe_2, WS_2), certain ones, like $NbSe_2$, also demonstrate superconductivity. The monolayers' distinctive features, including strong spin-orbit coupling and the absence of inversion symmetry, render them promising candidates for applications in spintronics and valleytronics.

1.2.1.1 Crystal Structure of MoS_2

TMDCs, or transition metal dichalcogenides, are a class of materials represented by the formula MX_2, where M belongs to the transition metal groups IV (such as Ti, Zr, Hf), V (Nb or Ta), or VI (Mo, W). X, on the other hand, stands for chalcogen, encompassing S, Se, or Te[28,34–36]. These elements combine to create the layered structural unit X-M-X, consisting of two hexagonal planes of chalcogen and one plane of metal atoms. In the formation of the bulk crystal in TMDCs, adjacent layers are connected by weak van der Waals interactions. There are three distinct crystal structures for TMDCs, determined by variations in stacking orders and metal atom coordination, as depicted in **Figure 1.6b**. Among these, the 2H structure is the most stable. In the 2H stacking, the ABA structure is followed in the c-direction, with two layers per repeated unit, denoted by 2H indicating hexagonal symmetry. The 3R structure possesses rhombohedral symmetry, trigonal prismatic coordination, and three layers per repeated unit, denoted by 3. This phase is relatively uncommon compared to the other two. The octahedral 1T phase of TMDC is a metallic metastable polymorph

with ABC stacking. The 1T phase can be induced through alkali-ion intercalation techniques or strain engineering in van der Waals heterostructures. However, it gradually transitions into the 2H phase with heating or over time[37]. The 1T phase is characterized by tetragonal symmetry denoted by T and one layer per repeated unit denoted by 1. It exhibits diamagnetic properties and is an indirect bandgap semiconductor with characteristics comparable to the 2H structure.

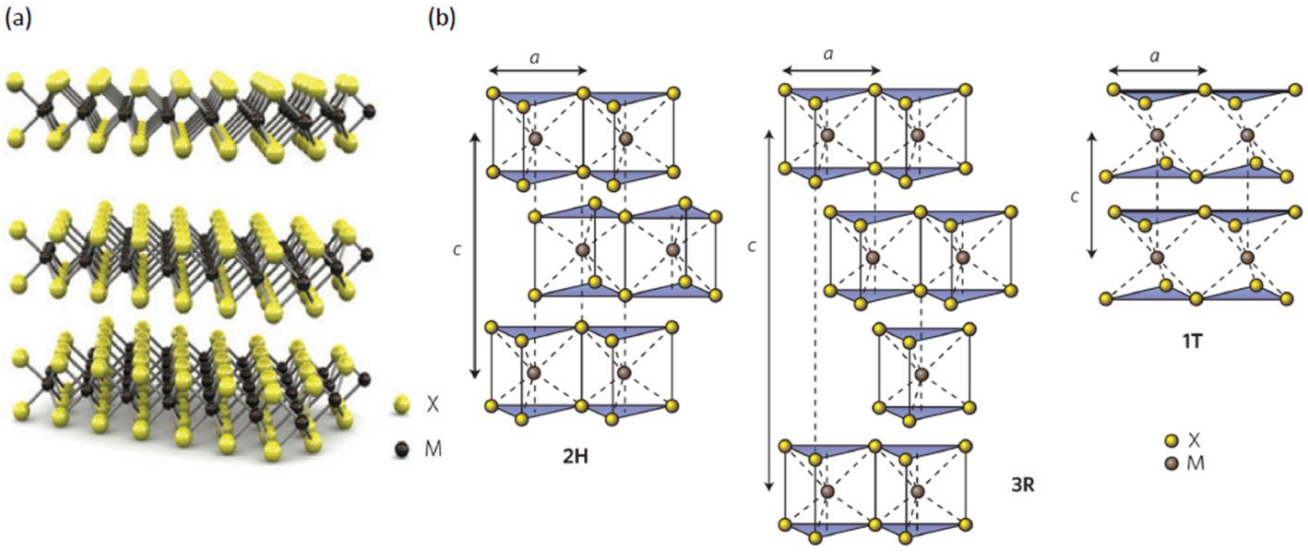


Figure 1.6. *(a) A three-dimensional schematic illustration of the MX_2structure, showing the metal atoms (M) and chalcogen atoms (X). (b) Schematic structures with different phases: 2H (hexagonal symmetry, two layers per repeat unit, trigonal prismatic coordination), 3R (rhombohedral symmetry, three layers per repeat unit, trigonal prismatic coordination) and 1T (tetragonal symmetry, one layer per repeat unit, octahedral coordination). (Adopted from ref. [37])*

1.2.1.2 Electronic Band Structure

TMDCs that are semiconductors show a direct bandgap in the monolayer and an indirect bandgap in the bulk. The primary cause of the observed photoluminescence from monolayer MX_2, which has made optoelectronic applications possible, is the direct bandgap[38,39]. First-principles calculations, tight-binding approximations, and measurements are used to determine the band structures of bulk and monolayer MX_2. DFT calculations show that the bulk crystal's valence band maxima are located at Γ-point. It is an indirect bandgap semiconductor because the conduction band minima are located at the Q-point (halfway between Γ and K). The theoretical analysis shows that the electronic states near the K-point are caused by localised d-orbitals of W (Mo) atoms, which are unaffected by interlayer coupling because they are sandwiched between Se (S) atoms.

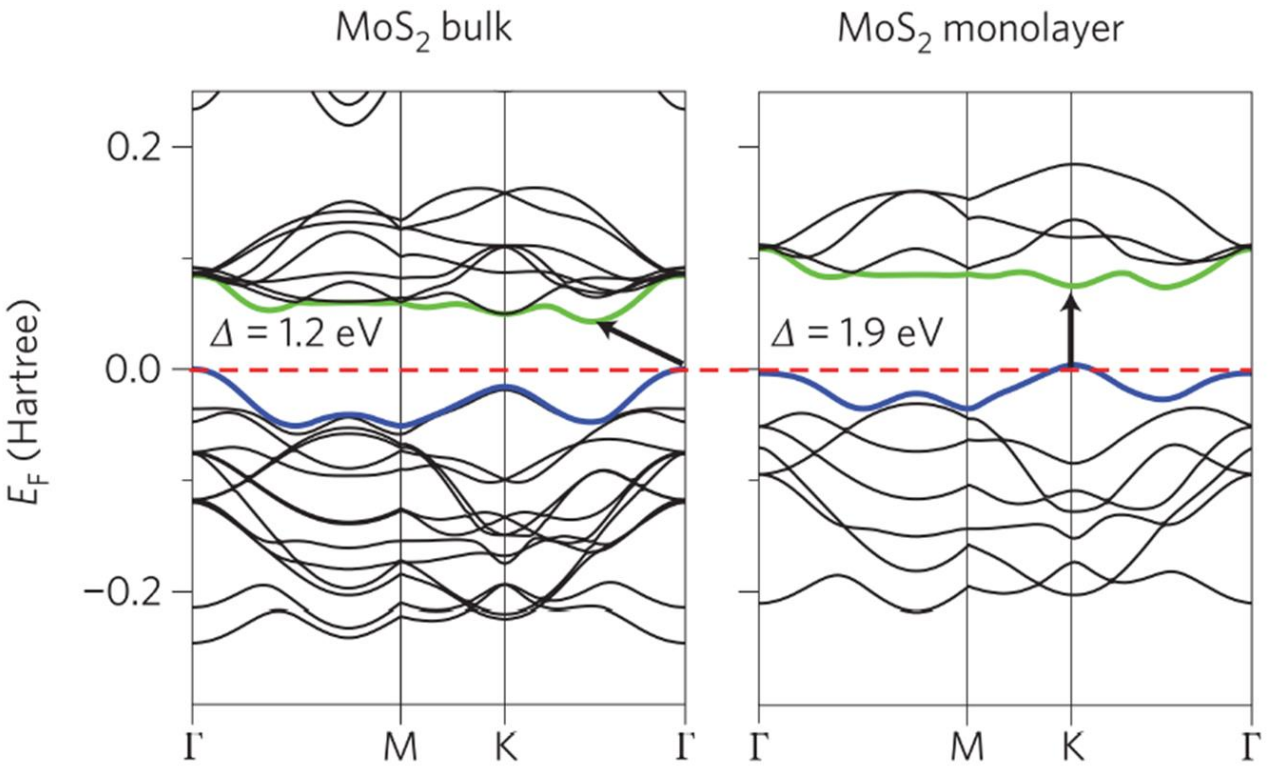


Figure 1.7. *Calculated band structure of bulk and single layer MoS2 using first principle DFT calculation.*

However, the states near the Γ-point are sensitive to interlayer interactions and arise from the p_z--orbitals of the Se (S) atoms and the d-orbitals of the W (Mo) atoms. As a result, as the layer numbers change, the direct excitonic states near the K-point remain relatively unchanged, but the transition at the Γ point shifts significantly from indirect to direct. With decreasing layer numbers, all MoX_2 and WX_2 compounds are expected to undergo a similar indirect-to-direct bandgap transformation. **Figure 1.7a** and **1.7b** shows the calculated band structure of bulk and monolayer MoS_2.

1.2.1.3 Vibrational properties of MoS_2

The key Raman peaks in MoS_2 include the in-plane E^1_{2g} and E_{1u} phonon modes, along with the out-of-plane A_{1g} mode[40,41] (refer to **Figure 1.8a**). When the layer thickness decreases, the A_{1g} mode frequency of MoS_2 around 406 cm^{-1} decreases, while the frequency of the E^1_{2g} mode around 382 cm^{-1} increases (see **Figure 1.8b**). These shifts in peak positions enable Raman spectroscopy to accurately assess layer thickness. The shifts result from neighboring layers affecting the

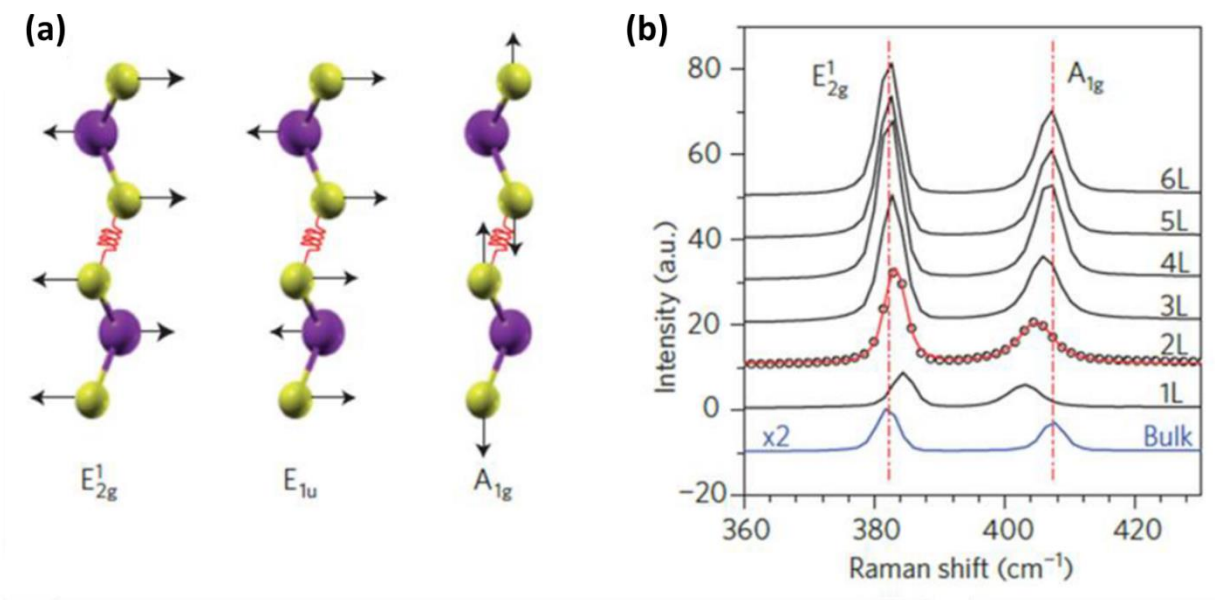


Figure 1.8. *(a) The in-plane phonon modes E^1_{2g} and E_{1u}, as well as the out-of-plane phonon mode A_{1g} of $MoS_2$are depicted schematically (analogously for WS_2). (b) Thickness-dependent Raman spectra for MoS_2. (Adopted from ref. [40])*

effective restoring forces on atoms and an enhanced dielectric screening of long-range Coulomb interactions. For instance, in monolayer MoS_2, the E^1_{2g} and A_{1g} modes are situated at 385 cm^{-1} and 404.5 cm^{-1}, respectively, with a difference of approximately 19.5 cm^{-1}. The A_{1g} mode experiences a blue shift (stiffening) with an increase in the number of layers, while the E^1_{2g} mode undergoes a red shift (softening). Consequently, for the bilayer, this shift becomes 22.5 cm^{-1}. Beyond four layers, no discernible changes occur, and the values converge to the bulk crystal value of 26 $cm^{-1,}$. These observations offer a straightforward and reliable means of determining layer thickness, widely applied in MoS_2 research.

1.2.2 Black Phosphorus (BP)

1.2.2.1 Crystal Structure of BP

Layered black phosphorus (BP) represents an elemental crystalline semiconductor composed solely of phosphorus atoms. The atomic structure of 2D BP, illustrated in **Figure 1.9a**, reveals that each phosphorus atom covalently bonds with three adjacent phosphorus atoms, creating a puckered hexagonal crystal structure[42,43]. This distinctive puckered BP crystal structure results in reduced symmetry, giving rise to unique angle-dependent optical and electronic properties. In the monolayer BP, there exist two distinct P–P bonds. One bond connects two nearest phosphorus

atoms within the same plane, with a bond length of 0.2224 nm. The other bond links two phosphorus atoms between the top and bottom layers, with a bond length of 0.2244 nm. This observation implies that two atomic layers come together to form the monolayer BP. The layer-to-layer distance measures approximately 0.53 nm, and the lattice constant in the z-direction is 1.05 nm. When examining the BP structure along the z-direction from a top view, it exhibits a hexagonal pattern featuring two types of bond angles: 96.3° and 102.1°.

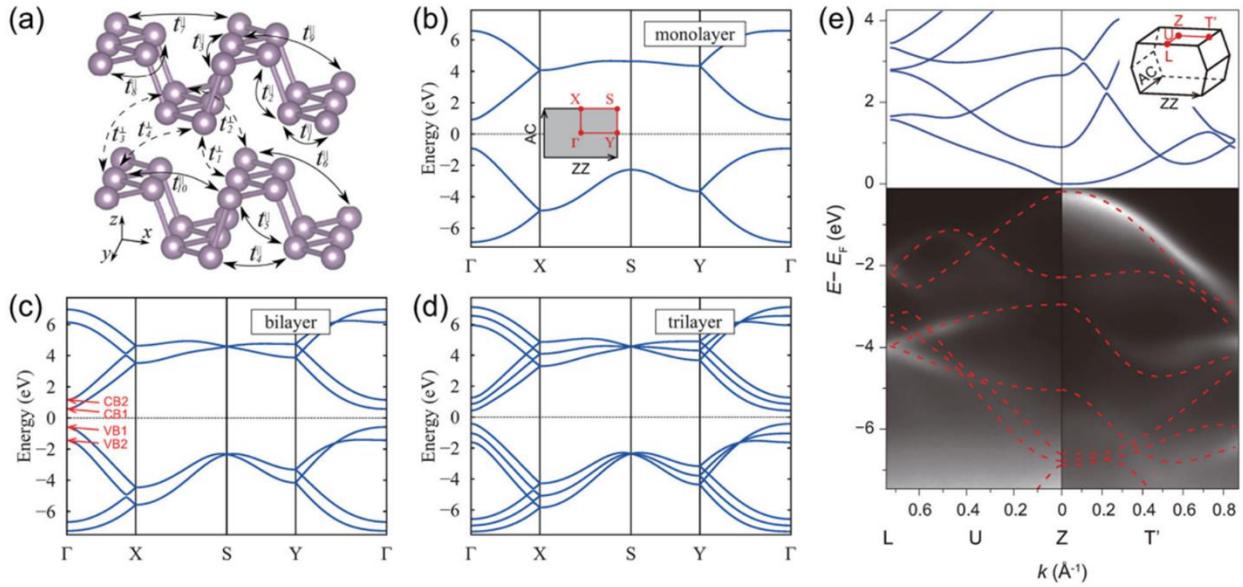


Figure 1.9. *(a) Schematic of the intra-layer and inter-layer hopping parameters in the tight-binding model. (b, c, d) Calculated band structures of monolayer, bilayer, and tri-layer BP, respectively. The 2D Brillouin zone is illustrated in the inset of (b). (a)–(d) Reproduced with permission.[42] Copyright 2015, American Physical Society. e) Band structure of bulk BP obtained by ARPES measurements, with the calculated bands (solid and dashed lines) superimposed on its top. The 3D Brillouin zone is illustrated in the inset. Reproduced with permission [43] Copyright 2014, Springer Nature*

1.2.2.2 Band structure of BP

Experiments[43] and theoretical calculation[42] reveal that, black phosphorus in its monolayer form is a direct band gap semiconductor. The minimum of the conduction band (CBM) and the valance band maximum (VBM) were identified at the Γ point of the 2D Brillouin zone. In the bilayer BP, the introduction of interlayer coupling results in a sharp reduction of the direct bandgap at the Γ point compared to the monolayer. In N-layer BP, the bandgap experiences further decrease due to robust interlayer couplings. Particularly intriguing is the splitting of the conduction band (CB) and valence band (VB) into N pairs of subbands, resembling transitional quantum wells (QWs).

Remarkably, these split conduction and valence subbands share a common origin in terms of the atomic orbitals as depicted in **Figure 1.9.**

1.3 Electrical transport in 2D materials

1.3.1 Electrical transport in Graphene

Graphene, as the first 2D material, has sparked considerable interest in the scientific community. Extensive experimental and theoretical research has focused on understanding its electronic transport characteristics in field-effect geometry. Graphene is produced via several methods such as mechanical exfoliation, chemical vapor deposition (CVD), epitaxial growth, etc. and FETs are fabricated on SiO_2/Si^{++} substrate, where Si^{++} acts as a back gate. Electrical contacts on the graphene flakes are formed using electron-beam lithography, photo lithography, or shadow masking. Following this, a layer of Ti/Au is deposited to metallize the contacts. The resistance (R) in graphene channel can be modulated by tuning the carrier density (n) through the application of gate voltage. The typical Resistance (R) vs Gate voltage (V_{bg}) characteristics show a peak in the resistance where the number of electrons and holes become equal leading the charge density effectively to be zero, termed as "Charge Neutrality Point (CNP)". The typical transfer characteristics of a graphene transistor is shown in **Figure 1.10b**. For single layer device, this is the point in the dispersion curve where the DOS goes to zero and called the "Dirac point" (V_D). In the majority of substrate devices, the charge neutrality point (CNP) is not consistently observed at 0 V_{bg}; instead, it tends to shift towards the negative or positive side. This shift is attributed to unintentional doping originating from the substrate or external adsorbents present on the surface[25,44]. The mobility of a graphene device can be calculated from Drude model using the relation,

$$\mu = \frac{\sigma}{ne} \quad \text{..... (1.11)}$$

Where, σ is the conductivity, e is the electronic charge, and n is the charge carrier density.

The carrier density (n) and the conductivity (σ) can be calculated using the following relation:

$$n = \frac{C_{bg}}{e}\left(V_{bg} - V_D\right) \quad \text{..... (1.12)}$$

$$\sigma = \frac{1}{\rho} = \frac{L}{RW} \quad \text{..... (1.13)}$$

Where C_{bg} is the oxide capacitance, V_{bg} is the back gate voltage, L and W are the length and width of the sample.

The device's optimal performance relies on achieving the ideal condition with n = 0. However, the presence of charge inhomogeneity[45], stemming from either substrate-induced trap charges or the strain caused by the roughness and lattice mismatch between the graphene and substrate[46,47], poses a significant obstacle. These factors contribute to an environment where attaining the desired n = 0 condition becomes challenging. Consequently, the quality of the device is compromised, emphasizing the need for strategies to address and mitigate these issues for enhanced device performance. In addressing substrate-induced inhomogeneity, researchers have experimented with

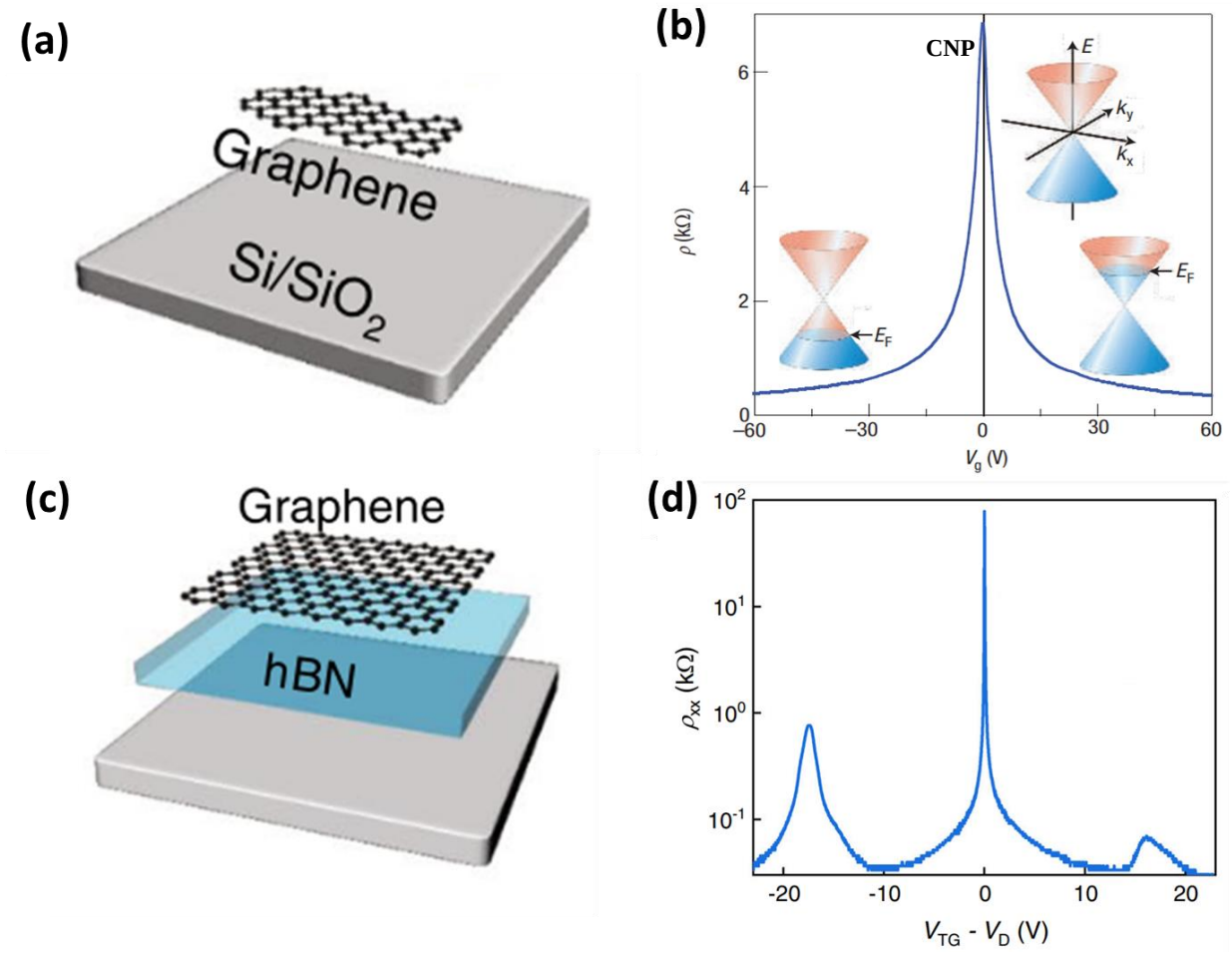


Figure 1.10. *Device structure and R-V_{bg} characteristics of a graphene exfoliated on (a), (b) SiO_2 substrate and (c), (d) on hBN substrate showing a huge increase in mobility and multiple Dirac points due to Moiré lattice. (Adopted from ref. [49])*

suspending graphene devices through the selective etching of the SiO_2 substrate[3,17]. This approach successfully mitigated the issue, revealing a notable improvement in electron mobility. However, the suspended devices exhibited considerable fragility, an inability to be doped to high carrier densities, and susceptibility to substantial strain.

Placing graphene on a hexagonal boron nitride (hBN) substrate significantly enhances device quality due to the minimal lattice mismatch and reduced charge inhomogeneity characteristic of the hBN substrate. In devices formed on this substrate, an impressive mobility of the order of 10^6 V/cm^2 has been observed (**Figure 1.10d**). Additionally, the slight lattice mismatch between graphene and hBN induces the formation of Moiré patterns, providing a platform to observe diverse and intriguing physical phenomena[4,48,49].

1.3.2 Electrical transport in 2D semiconductors

In 2011, Andras Kis's group successfully delved into the electronic properties of single-layer MoS_2 FET[5], revealing its n-type semiconductor characteristics (**Figure 1.11a**). Subsequently, other research groups observed ambipolar conduction in MoS_2 through ionic liquid or high-dielectric gating[50,51]. Despite the remarkable on/off ratio ($\sim 10^8$) and subthreshold swing (74 mV per decade) exhibited by MoS_2 transistors, their mobility on Si/SiO_2 substrates remained low (**Figure 1.11a**), presenting a limitation for transition metal dichalcogenide (TMDC) materials.

Further investigations highlighted that the inclusion of a high-κ dielectric significantly enhanced mobility by orders of magnitude, suggesting the effective screening of charged impurity scattering. This improvement indicated the potential of high-κ dielectric environments to mitigate the impact of charged impurity scattering on ultrathin MoS_2 transistor transport properties[52]. Short-range and electron-phonon scattering were identified as crucial factors influencing the transport mechanism. Despite the notable n-type behavior of MoS_2 transistors, there is a crucial need to explore p-type transistors to optimize TMDC-based CMOS technologies. The challenges posed by Fermi pinning near the valence band and the mobility limitations underscore the importance of ongoing research to unlock the full potential of TMDC materials in semiconductor applications[28,53,54]. Recently, Black phosphorus (BP)[8,42], an elemental semiconductor, has exhibited its efficacy as a channel material capable of yielding high-performance Field-Effect Transistors (FETs). Notably, even in the configuration of few-layer BP transistors, it has demonstrated a noteworthy carrier mobility

value of approximately 1000 cm^2/Vs at room temperature. This performance is in stark contrast to other Transition Metal Dichalcogenides (TMDCs). Black phosphorus being a narrow band gap semiconductor, it is easier to control the carrier type from p to n type material resulting into an ambipolar characteristics. Contrary to the general trend observed in TMDCs, black phosphorus

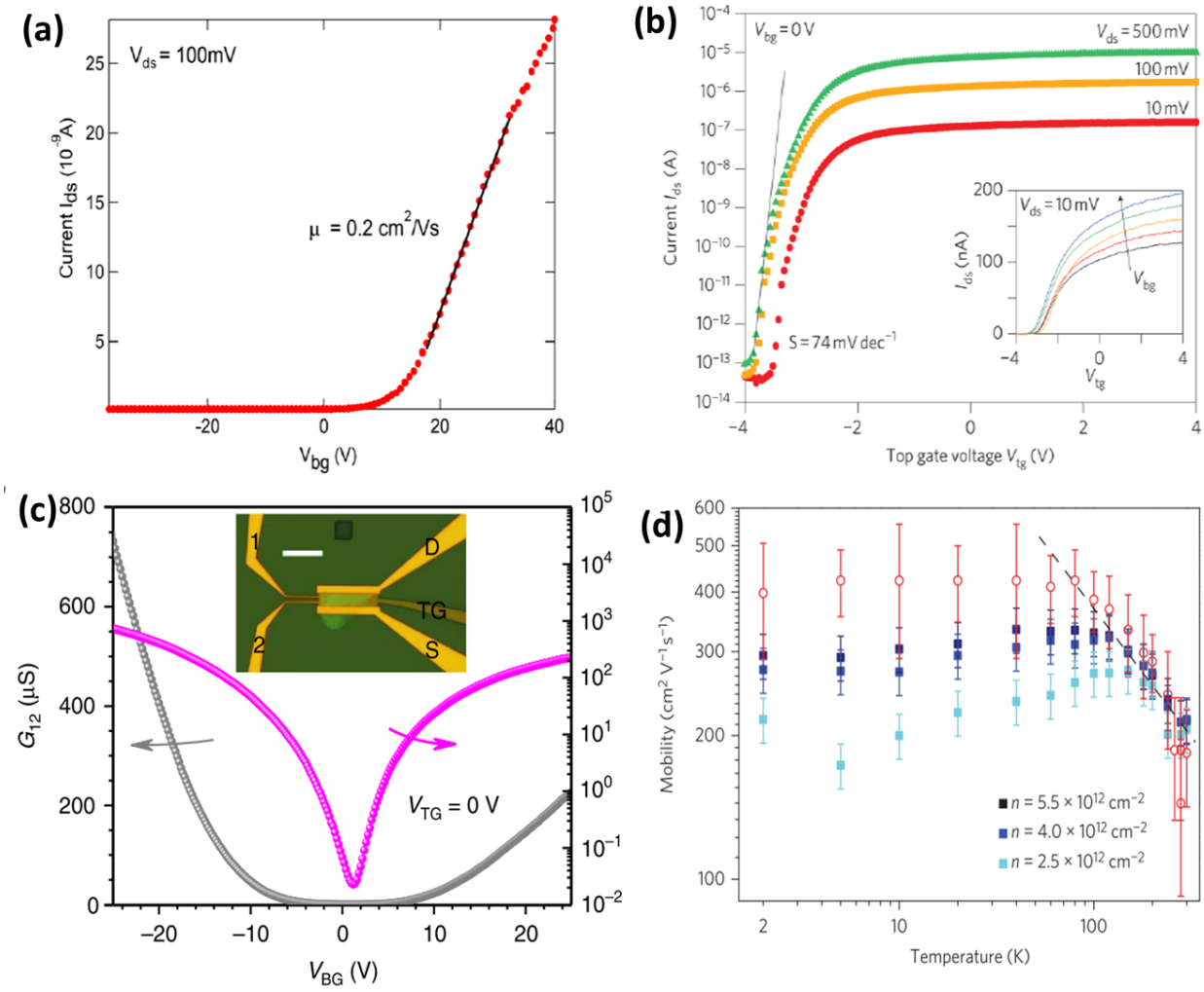


Figure 1.11. *(a) Transfer characteristics of Monolayer layer MoS_2 transistor on SiO_2 substrate showing n-type behavior. (b) Extremely high (10^8) on/off ratio in single layer MoS_2 transistor. (c) High mobility ambipolar transport in few layer Black Phosphorus FET. (d) Field-effect mobility (red open circles) and Hall mobility (filled squares, three different values of n) as a function of temperature on a logarithmic scale. (Adopted from ref. [5],[51],[42])*

has shown the ability to partially preserve the bulk carrier mobility value when reduced to a few-layer form. This distinct characteristic further underscores the unique potential of black phosphorus in the realm of electronic devices.

1.4 Disorder and Scattering mechanism in 2D materials

In theory, graphene was anticipated to exhibit ballistic transport, particularly at low temperatures when the phonon contribution is suppressed. Yet, in practice, the transport properties of graphene were found to exhibit more diffusive behavior rather than ballistic, aligning with semi-classical Boltzmann transport equations. In the case of 2D semiconductors like MoS_2, WS_2, it has been observed that the mobility of these devices is considerably lower than the theoretically predicted values. It was also observed that presence of high-k dielectric can improve the mobility by orders of magnitude. This indicates a possible role of charged impurity scattering on the transport properties of ultrathin MoS_2 transistor which quenches in the presence of a high k -dielectric environment. This discrepancy arises from the presence of various types of disorder and scattering mechanisms, stemming from both internal and external factors. Internal factors include short-range scatterers due to lattice defects and acoustic phonons. Conversely, external sources of scattering, such as charged impurity scattering caused by oxide trap charges, substrate roughness, and substrate polar phonons, contribute to the deviation from theoretical predictions. In this context here, in this section, we have discussed the various Scattering mechanism and the sources of disorder present in the 2D materials.

1.4.1 Long range charge impurity scattering

Initially, due to its linear bandstructure, it was believed that the conductivity in graphene might remain unaffected by carrier density[55]. However, experimental observations contradicted this notion, revealing that conductivity exhibits a linear relationship with carrier density, deviating from the Dirac point. This discrepancy was elucidated by introducing charged impurities within or in close proximity to the graphene channel[26,56–59]. To experimentally investigate the impact of these charged impurities, intentional doping of the graphene channel with potassium ions was conducted. The results showed a shift of the Dirac point towards higher negative gate voltages with increasing doping levels, accompanied by a more linear conductivity with density. Presently, it is well-established that in the case of graphene on a SiO_2 substrate, the dominant factor influencing transport is charged impurity scattering arising from oxide trap charges.

One effective approach to mitigate the impact of long-range scattering is to suspend the graphene channel [60]. This suspension has led to a significant increase in device mobility, unveiling intriguing phenomena such as the fractional quantum Hall effect[17]. Despite these advancements, suspended

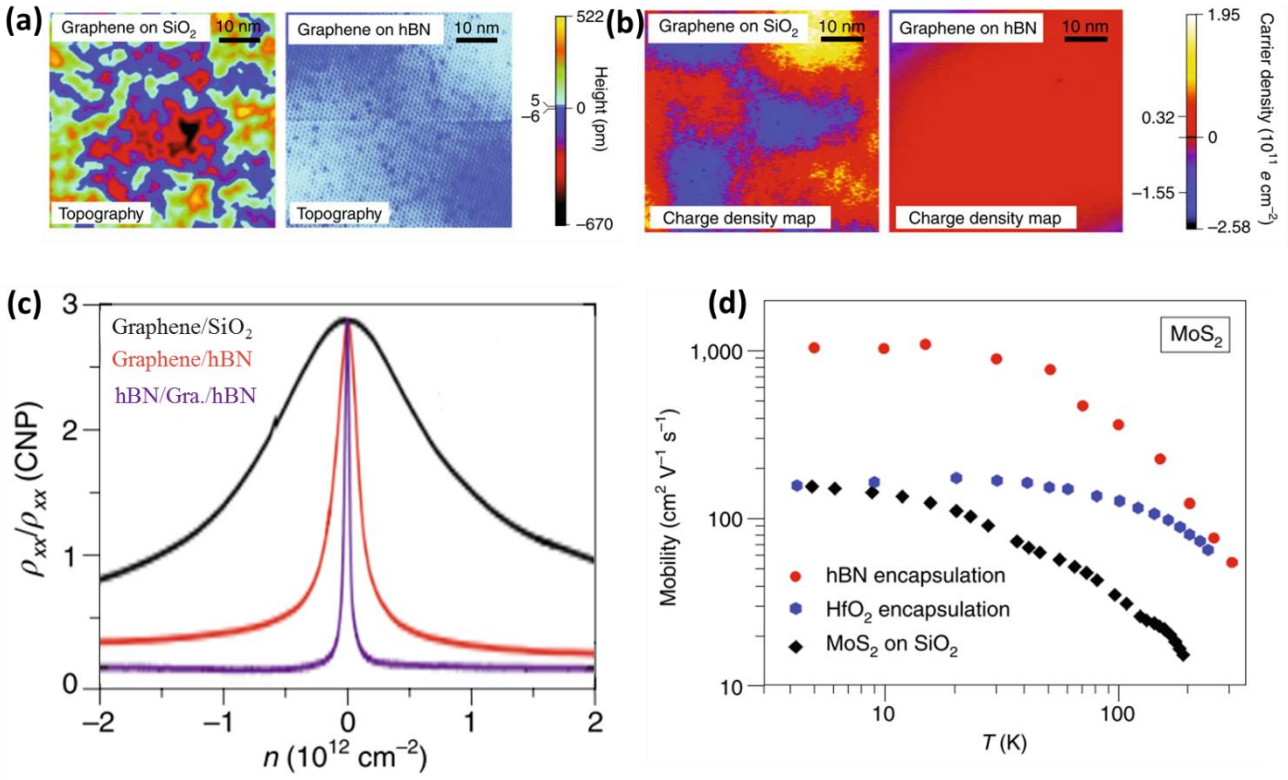


Figure 1.12. *(a) Comparison of STM topography (a) and charge density maps (b) for graphene on hBN versus graphene on SiO_2. (c) Normalized resistivity versus gate-induced charge density for graphene/SiO_2, graphene/hBN, hBN/Graphene/hBN substrate, showing the dramatic decrease in Dirac peak width due to reduction of disorder-induced broadening. (d) Experimental observation of mobility versus temperature on a log scale for monolayer MoS_2 on SiO_2, HfO_2, and encapsulated in hBN.*

devices encounter limitations, including constraints on gate-induced charge density, weak gate capacitance, challenges in handling complex geometries, and a lack of flexibility for stacking multilayer structures.

The utilization of hBN substrates for graphene presents clear advantages compared to SiO_2 substrates. Analysis through STM topography and charge density maps[61] reveals that the rms roughness in the in the surface charge density for the graphene/hBN (2.3×10^{10} cm^{-2}) is markedly lower than that observed for graphene/SiO_2 (8.2×10^{10} cm^{-2}). Both roughness and charge density inhomogeneity are significantly reduced on hBN substrates, positioning hBN as an ideal candidate for supporting 2D materials. Subsequently, there is a dramatical change in the width of the peak of the resistance vs. gate voltage curve near the charge neutrality point as shown in **Figure 1.12**. Like graphene, monolayer TMDCs experience significant extrinsic disorder when placed on SiO_2

substrates. Two primary strategies have been employed to mitigate the impact of this disorder: (i) the deposition of high-κ dielectric materials such as HfO_2 or Al_2O_3. These materials not only screen charged impurities but also reduce charged impurity density through surface passivation. (ii) Encapsulation within hBN, which introduces a greater distance between the conducting channel and the SiO_2 surface. This spatial separation helps minimize the effects of charge disorder.

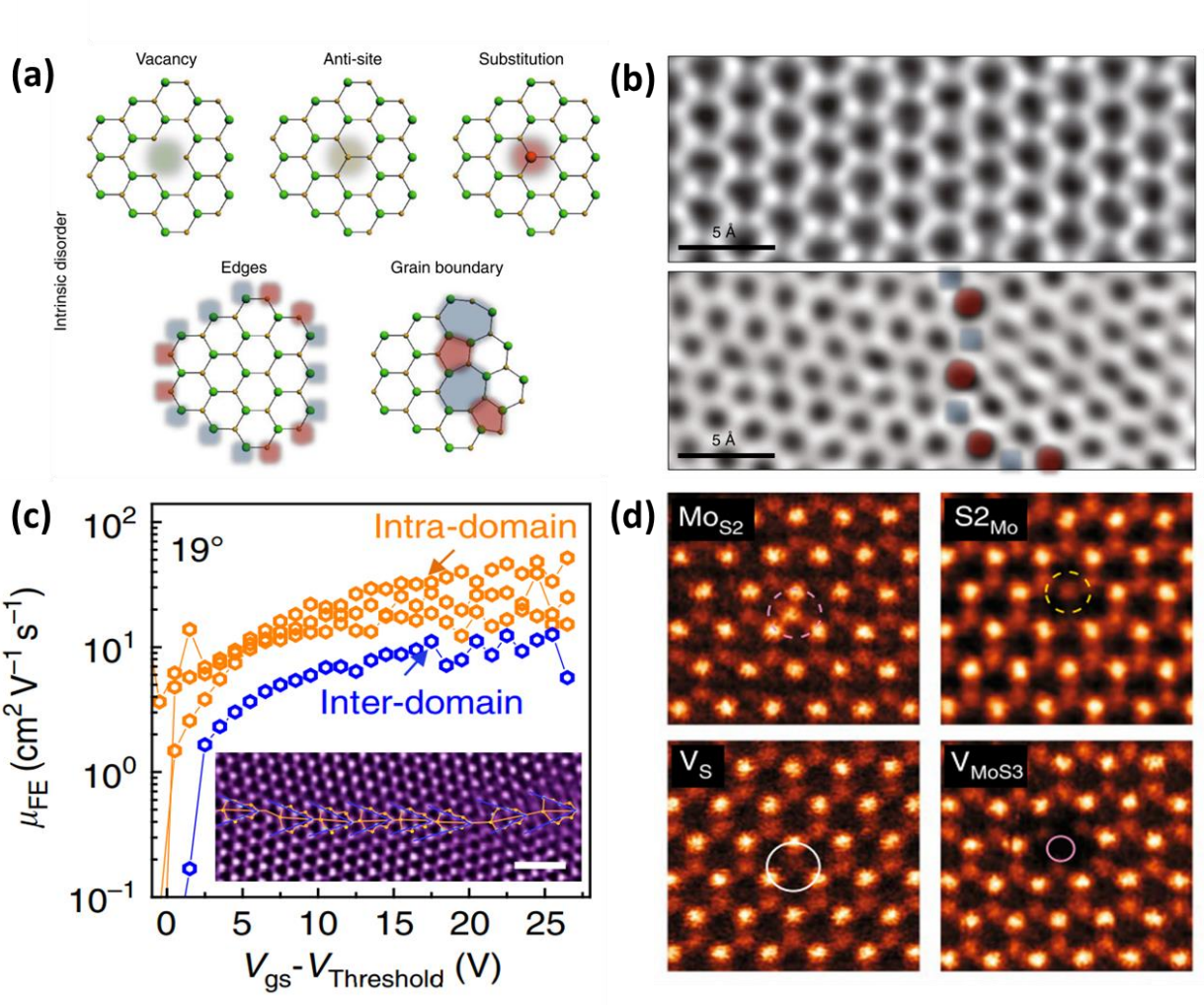


Figure 1.13. *(a) Schematic of the different type of intrinsic disorder present in 2D system. (b) The top image depicts an aberration-corrected annular dark-field STEM view of the graphene lattice, highlighting the absence of defects. In contrast, the bottom image reveals a grain boundary in CVD-grown graphene. (c) The electrical performance of intra-domain regions consistently exhibits higher mobility in comparison to the inter-domain region of a MoS_2 device. An inset features a STEM image illustrating the boundary. (d) STEM images are employed to emphasize each significant defect in MoS_2.*

Additionally, charge disorder originating from the SiO_2 surface can be further addressed by incorporating a conducting back-gate beneath the hBN, effectively screening the undesirable effects, and enhancing the overall performance of monolayer TMDs. All the measurement and findings indicate that the substrate plays a very important role in determining the transport properties of 2D materials.

1.4.2 Short range scattering

Short-range scatterers in 2D materials, such as crystal defects, vacancies, external neutral atoms, and topological disorder, contribute to its characteristics. In samples with relatively high mobility, a sub-linear behavior was noted in the high-density regime[62]. This observation suggests that these samples may have a minimal presence of charged impurities or that long-range scattering is screened at high density, allowing short-range scattering to govern charge transport. As a consequence of short-range scattering, conductivity attains a limiting value, causing mobility to become inversely proportional to carrier density. Intrinsic disorder arises from various sources, illustrated in **Figure 1.13a** for a hexagonal lattice but relevant to all 2D crystals. These sources encompass atomic defects like vacancies, anti-sites, substitutions, edges, and grain boundaries. Particularly in large-area, poly-crystalline monolayer films, such grain boundaries can exert a significant influence on the materials' properties. In the case of graphene, the conductivity may decrease by a factor of three due to transport across a single grain boundary[63,64]. In transition metal dichalcogenides (TMDCs), grain boundaries induce local strain, impacting the bandgap in a manner dependent on the tilt angle between the grains[65].

1.4.3 Phonon scattering

Lattice vibrations serve as unavoidable sources of scattering, exerting a notable influence on transport in the vicinity of room temperature. They act as an inherent scattering source, constraining mobility at finite temperatures in the absence of all extrinsic scattering sources. Generally, three distinct types of phonon scattering are examined: intra-valley acoustic and optical phonon scattering, triggering electronic transitions within a single valley; and inter-valley phonon scattering, provoking electronic transitions between different valleys. Yet, recent experiments disclose that remote polar optical phonons in the substrate (SiO_2) adversely impact carrier mobility[61,66,67]. The intricate temperature dependence of Hall mobility at various densities for

single, bi, and tri-layer graphene was explored by Zhu et.al[68] , illustrated in **Figure 1.14**, with the findings elucidated by considering both charge impurity and phonon scattering.

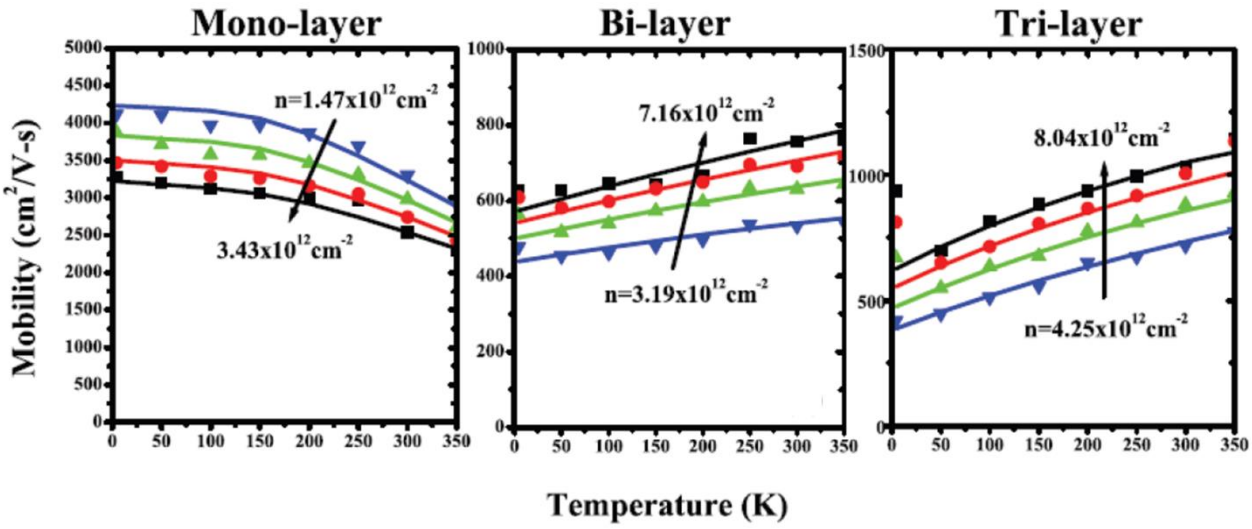


Figure1.14. *Hall mobility as a function of temperature for different hole densities in monolayer graphene, BLG, and tri-layer graphene respectively. The symbols are the measured data and the lines are fits. Adapted from ref. [68]*

In case of 2D semiconductors like in case of MoS_2, at elevated temperatures, phonon scattering assumes a significant role, while at lower temperatures, where phonon interaction is limited, charge scattering takes precedence in the scattering process[69]. The figure illustrates that at temperatures below 200 K, the mobility of un-encapsulated MoS_2 experiences a decline with decreasing temperature due to Coulomb impurity scattering (**Figure 1.15a**). Beyond 200 K, the mobility diminishes with rising temperature, following a relationship $\mu \sim T^{-1.4}$ due to electron-phonon scattering[69], albeit slightly smaller than the theoretical calculation[70] ($\mu \sim T^{-1.6}$). Radisavljevic et.al.[52] Demonstrated that the mobility becomes temperature-independent below 30 K, with a reduction in the exponent from 1.4 to 0.78 at high temperatures when a high-k dielectric is deposited on top of the MoS_2 (**Figure 1.15b**). This suggests screening of impurity scattering at low temperatures and suppression of phonon scattering at high temperatures due to the high-k dielectric.

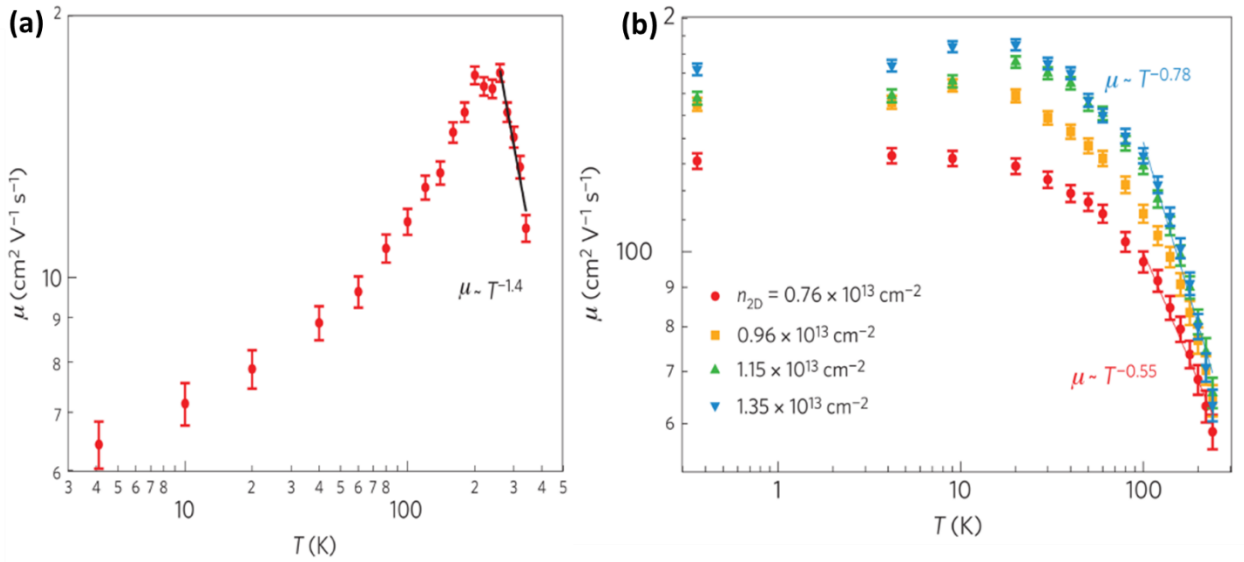


Figure 1.15. *(a) Temperature dependence of mobility μ for a single layer un-encapsulated MoS_2 FET, showing charged impurity scattering regime at low temperature and phonon scattering regime at high temperature. (b) μ vs T graph of dual gated single layer MoS_2, showing a saturation at low temperature, and suppression of phonon scattering at high temperature due to dielectric screening. Adopted from ref. [69],[52].*

1.4.4 Localization and trap state

It has been observed by various scientific groups that the electronic states in TMDC's are highly localized, where the electronic transport is dominated by the hopping of electrons between the localized states. In a strongly disordered system, the electronic wave functions exhibit strong localization at the disorder potentials. The amplitude of the electronic wave function decays exponentially as it moves away from the site of localization. This confinement occurs within a characteristic length scale ξ, commonly referred to as the localization length. At T = 0 K the electrons cannot move from one site to another due to unavailability of sufficient thermal energy, but at a finite temperature they can hop between the localized sites. This hopping can be carried out by various mechanism, and are discussed below:

- **Nearest Neighbor Hopping (NNH):** At elevated temperatures, wherein a considerable multitude of phonons becomes accessible to the system due to thermal fluctuations across a broad energy spectrum, the phenomenon of Nearest Neighbor Hopping (NNH) transpires. In this scenario, electrons can do transition from one site (E_i) to another site (E_j) by either absorbing or emitting phonons. The likelihood of such electron hopping is most pronounced between nearest neighbors, primarily owing to the substantial overlap of their wave functions.

This characteristic defines the process as nearest neighbor hopping[71]. In NHH the temperature dependent conductivity shows activated behavior

$$\sigma = \sigma_0 e^{(E_j - E_i)/K_B T} \quad \text{..... (1.14)}$$

- **Variable Range Hopping (VRH):** VRH manifests at extremely low temperatures, characterized by a thermal energy bandwidth (k_BT) that narrows down beyond the extent of the energy distribution of localized states. In this scenario, an electron has the capability to jump from one site to another within the energy range scale, disregarding the spatial distance between the sites. Consequently, this hopping process is labeled as variable range hopping. According to Mott's calculation, the expression for the probability of an electron to hop from one site (R_i, E_i) to another site (R_j, E_j) is as follows:

$$P_{ij} \sim \exp\left(-\frac{2R}{\xi} - \frac{\Delta}{k_B T}\right) \quad \text{..... (1.15)}$$

Where $R = (R_j - R_i)$ and $\Delta = E_j - E_i$. Here the density of states is assumed to be slowly varying at the Fermi level. The first term in the above equation denotes the tunneling probability between the two sites while the second term is related to the transition probability due to thermal activation. The more general form of the temperature dependent conductivity is given by[6,72]:

$$\sigma = \sigma_0 \exp[-\left(\frac{T_0}{T}\right)^{\frac{1}{d+1}}] \quad \text{..... (1.16)}$$

Here, T_0 is the correlation energy and d is the dimensionality of the system.

1.5 Resistance Fluctuation or Noise

Electrical transport involves a crucial parameter known as 'resistance fluctuations' or 'electrical noise', inherent in any materials or devices due to various fundamental reasons. The examination of noise holds significance not only from a fundamental perspective but also in terms of practical applications. The resistance (R) of a material characterizes its time-averaged transport properties. On the other hand, resistance fluctuations manifest as dynamical variations $\Delta R = R(t) - < R >$

around the time-averaged mean value < R >. Noise emanates from fluctuations in microscopic entities, providing a direct means to investigate the system's physical properties at the microscopic level.

1.5.1 Types of Noise

There are three types of noise.

- **Thermal Noise-** The phenomenon commonly referred to as 'Nyquist noise[73],' also known as 'Johnson noise' or 'thermal noise,' is a manifestation of the fluctuation-dissipation theorem. This principle relates the thermal fluctuations in a system to the dissipation of energy. In the context of a resistor with a value of R maintained at a temperature T, the power spectral density (PSD) of thermal noise is expressed as

$$S_V(f) = 4k_B TR, \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1.17)$$

  where k_B is the Boltzmann constant. Notably, the spectral power $S_V(f)$ is independent of frequency, often termed 'white noise,' and is unaffected by the current flowing through the resistor or the material properties of the resistor. This characteristic makes thermal noise less versatile as a tool, except in situations where it can serve as a measure of the effective electron temperature. Despite its limitations, understanding and accounting for Nyquist noise are essential in various applications, particularly in cases where precise measurements or signal integrity considerations are critical.

- **Shot Noise:** Shot noise[74] emerges from the discrete nature of charge carriers within a conductor, and its mathematical representation is given by

$$S_I(f) = 2q\langle I\rangle, \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1.18)$$

  where q represents the charge of the carrier and ⟨I⟩ denotes the average current flowing through the conductor. Similar to thermal noise, shot noise is also characterized as white, meaning it exhibits a frequency-independent power spectral density. In the realm of mesoscopic physics, shot noise assumes particular significance as it provides a direct experimental means of measuring the charge and statistics of the current-carrying quasiparticles within a system. This

distinctive noise phenomenon becomes discernible primarily at low temperatures and high frequencies, where the effects of thermal noise and 1/f noise are significantly diminished. As a result, shot noise serves as a valuable tool in exploring and understanding the behavior of charge carriers in mesoscopic systems, offering insights into their statistical properties under specific experimental conditions.

- **1/f Noise:** Voltage fluctuations in a resistor carrying current often follow a power spectrum that scales as $\frac{1}{f^{\alpha}}$, with α approximately equal to 1. This characteristic noise, commonly referred to as '1/f noise' or 'flicker noise[75–77]' in the literature, is notable for its inverse proportionality to the volume of the sample between the measurement probes. As the sample size decreases, the noise sources' dimensions remain constant, leading to more pronounced fluctuations in the overall electronic transport. The spectral power of the voltage noise $S_V\ (f)$ exhibits a quadratic dependence on the applied bias, causing an increase above the thermal voltage when an appropriate bias voltage is applied. The prevalence of 1/f noise extends across various material systems[7578], including semiconductors, metallic and magnetic films[79], spin glasses[80], heterogeneous conductors, superconductors[81] in the normal state, tunnel junctions, electronic devices, and even applications like magnetic sensors and heartbeat monitoring. Beyond its practical applications, 1/f noise has proven instrumental in studying diverse physical phenomena such as structural phase transitions[79], magnetic domain wall motion[82], and many-body physics, including electron glasses and quantum transport in low-dimensional systems..

1.5.2 Theories of 1/f Noise

The manifestation of 1/f noise in solid-state systems is intricately linked to both the quality and purity of the sample. Numerous research groups have endeavored to model the origin of 1/f noise in solid-state systems throughout the course of time. Despite these efforts, a comprehensive and unified theory capable of directly explaining every aspect of its origin remains elusive to date. In the realm of condensed matter systems, the emergence of 1/f noise is often attributed to the relaxation of defects or groups of defects, each characterized by finite relaxation times. In the subsequent section, we will explain several important models that are relevant to the present thesis work.

1. Hooge's model:

The Hooge[83] mechanism serves as a phenomenological model tailored for homogeneous conductors, wherein the bulk of the material serves as the primary source of noise, distinct from contributions arising from the material's surface. At its core, the origin of the noise is rooted in fluctuations within the scattering cross-section in the channel. This model establishes an inverse relationship between the noise and the number of charge carriers present in the channel. The comprehensive Hooge relation is expressed as

$$S_V(f) = \gamma_H \frac{V^2}{Nf^\alpha} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1.19)$$

Where $S_V(f)$ represents the power spectral density of voltage fluctuations, γ_H is the Hooge parameter, V is the mean voltage drop, N is the number of charge carriers in the channel, f is the frequency, and α is the noise exponent typically approximating 1.

The Hooge parameter, γ_H serves as a crucial characterization of the noise magnitude within the channel. The resultant noise engenders a normalized spectral density of resistance, denoted as S_R/R^2, which scales inversely with the number density, approximating $S_R/R^2 \sim$ 1/n. Remarkably, this mechanism finds applicability across a diverse array of systems, including thin metal films, transition metal dichalcogenides, Graphene, carbon nanotubes, and other analogous materials[84–87].

2. McWhooter model:

McWhorter[88] introduced a model aimed at elucidating the 1/f noise behavior observed in Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). According to this model, the origin of 1/f noise in MOSFETs can be attributed to the sluggish trapping-detrapping processes occurring between the conduction channel and oxide traps situated at the oxide-semiconductor interface. This dynamic interplay results in fluctuations in the number density, which manifest as 1/f noise in the drain-source current (I_{dS}). The fundamental postulates of this model include the following: (i) Traps, characterized by a broad distribution in energy (E), are positioned in the oxide layer extending from the interface towards a depth (x) within the oxide. (ii) Carrier trapping and detrapping events alter the number of carriers in the channel without introducing any fluctuations in mobility. (iii) Electrons can elastically tunnel to trap states inside the oxide against the conduction band barrier height (ϕ_B) with a time constant $\tau = \tau_0 e^{\alpha x}$, where $\alpha = \sqrt{(2m\phi_B/\hbar^2)}$. The distribution of tunneling distances gives rise to the observed 1/f noise. In this model, the finite temperature (T) scenario implicates that trap states $k_B T N_t(E_F)$ around the Fermi energy (E_F)

predominantly contribute to the noise. This nuanced explanation provides valuable insights into the intricate processes governing 1/f noise in MOSFETs, particularly emphasizing the role of trapping-detrapping dynamics at the oxide-semiconductor interface. The total noise PSD can be calculated as

$$\frac{S_I(f)}{I_{DS}^2} = \frac{k_B T q^2 N_T(E_F)}{8WLn^2 e^2 f} \quad \text{..... (1.20)}$$

where, $N_T(E_F)$ is the oxide trap density near E_F and L, W are the length and width of the channel respectively. A distinct feature of this number fluctuation model is that $S_I/I_{DS}^2 \propto 1/n^2$, where n is the number density of carriers in the channel.

3. Dutta-Horn Model

This phenomenological model was first developed to explain the 1/f noise behaviour seen in metallic thin films [77]. It suggests that the genesis of 1/f noise is the slow relaxation of flaws and disorder in the film over the course of the experiment. According to the model, in the event that the system displays a single relaxation time (τ) with an exponential autocorrelation function $\phi(t) \sim e^{(-t/\tau)}$, a Power Spectral Density (PSD) with a Lorentzian distribution will follow

$$S(f) \sim \frac{2\tau}{1+(2\pi f\tau^2)} \quad \text{..... (1.21)}$$

If there is a distribution of time scales, $F(\tau)$, in the system, the total PSD can be written as

$$S(f) \propto \int_0^\infty \frac{2\tau}{1+(2\pi f\tau)^2} F(\tau) d\tau \quad \text{..... (1.22)}$$

If we assume $F(\tau) \sim 1/\tau$ over a range of $\tau_{min} \ll \tau \ll \tau_{max}$, then $S(f) \sim 1/f$ in the range $\tau_{max}^{-1} \ll f \ll \tau_{min}^{-1}$. Dutta-Horn model explains the activated kinetics of defects and disorder. The relaxation time is given by the product of the microscopic attempt time ($\tau_0 \sim \omega_D^-$, ω_D is the Debye frequency) and the exponential of the activation energy E for defect migration in the scale of $k_B T$. This gives

$$S(f,T) \propto \int_0^\infty \frac{2\tau_0 e^{\frac{E}{k_B T}}}{1+\left(2\pi f\tau_0 e^{\frac{E}{k_B T}}\right)^2} D(E) dE \quad \text{..... (1.23)}$$

When $D(E)$ slowly varies in the scale of k_BT, then $S(f) \sim 1/f^{\alpha}$.

4. Local interference Model

None of the previously discussed models successfully elucidates the coupling mechanism responsible for translating defect motion into experimentally observable resistance fluctuations. It has been demonstrated that the scattering of conduction electrons by structural defects[89], such as vacancies and interstitial defects, each acting as independent scattering centers particularly at elevated temperatures, plays a pivotal role in this context. The interference stemming from electrons scattered by various centers induces anisotropy in the resistivity tensor, and this anisotropy is contingent upon the distance between the scattering centers.

Building upon these premises, Pelz and Clarke[90] extended the argument by calculating alterations in the scattering cross-section associated with anisotropic defects as they undergo motion. This dynamic process results in changes in electron scattering rates, giving rise to resistance fluctuations characterized by a 1/f spectrum. Termed the 'Local Interference model,' this conceptual framework emphasizes the primary influence of electron interference occurring within a few lattice constants of each other. If the number density of mobile species in the system is denoted as nm, then the total noise emanating from all fluctuators can be quantified as

$$\left[\frac{<(\Delta R)^2>}{<R>^2}\right] = \frac{1}{N}\frac{n_m}{n}(nl_e\beta_c\Lambda_c)^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1.24)$$

Where N is the total number of atoms in the sample, $n = N/V$ the density of atoms, l_e the mean free path, Λ_c the average defect cross-section and β_c is the anisotropy parameter which denotes the effective 'scattering power' of various types of defects. This model is applicable at the high temperature limit where $L_\phi \ll l_e$.

5. Universal Conductance Fluctuation

The development of this model is grounded in the analogous concept of weak localization observed in disordered metallic systems. Specifically, at low temperatures, when the phase coherence length (L) exceeds the elastic mean free path ($L > l_e$), the electronic wave functions experience backscattering from impurities, leading to interference. This quantum mechanical interference proves highly susceptible to the spatial arrangement of impurities. The coherent superposition of

wave functions, vital for conductance, can undergo a significant alteration with even minor changes in disorder configuration, resulting in a shift in conductance on the order of e^2/h. This phenomenon is recognized as universal conductance fluctuation (UCF)[91] and manifests as 1/f noise at low temperatures. Experiments conducted on disordered metal films on Bi, Ag, and more recently on graphene have demonstrated that conductivity fluctuations can be attributed to UCF at low temperatures[92–94].

1.6 Functionalization of Graphene

Graphene properties include rapid charge transport, exceptional thermal conductivity, mechanical robustness, and flexibility. Given these distinctive attributes, Graphene stands out as a highly

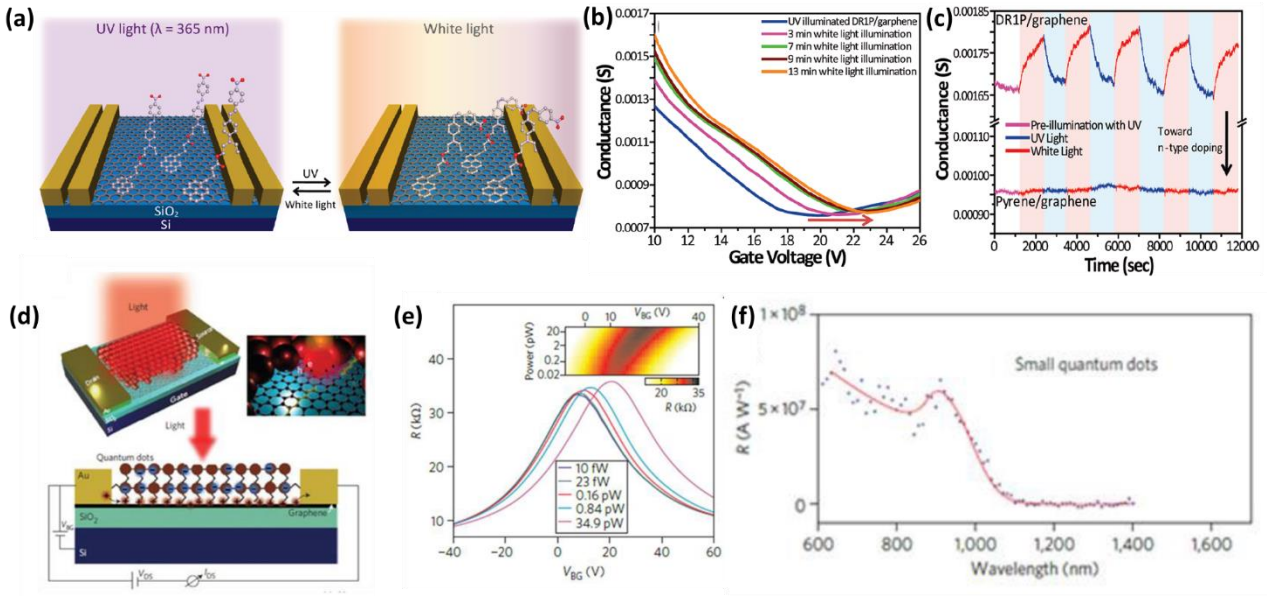


Figure 1.16. *(a) Graphene FET decorated with a derivative of Azobenzene molecular system which is sensitive to UV light. (b) Conductance as a function of gate voltage when the UV illuminated on the decorated devices. (c) Switching response as function of UV light exposure in the Azobenzene decorated graphene device. Graphene-quantum dots hybrid phototransistors. (d) Schematic of the hybrid device where PbS quantum dots coated on a graphene flake on a Si/SiO_2 substrate. (e) Resistance (R) as a function of back-gate voltage (VBG) of the hybrid device for increasing illumination intensities with λ= 500 nm. (f) Spectral photoresponse of two hybrid phototransistor devices with PbS quantum dot. Adopted from references [96],[99].*

promising material for a diverse array of applications in nanoelectronics, microelectronics, macroelectronics, and flexible electronics. Nevertheless, the lack of a bandgap in pristine graphene devices presents a significant hurdle as it prevents them from being switched off. This challenge

proves particularly formidable in the context of applications for digital electronic devices. Realizing the potential of graphene in electronics necessitates the precise manipulation of its electronic properties. Doping, a conventional strategy for controlling the electronic characteristics of semiconducting materials, is also applicable to graphene. One effective approach to achieve graphene doping involves the substitution of carbon atoms in the graphene lattice with heteroatoms. While substitutional doping results in a stable system, it introduces defects that disrupt the honeycomb structure of graphene. To overcome this challenge, the sensitivity of graphene to local perturbations can be exploited, such as those induced by physically adsorbed gaseous molecules. This process is inherently reversible, allowing for dynamic adjustments.

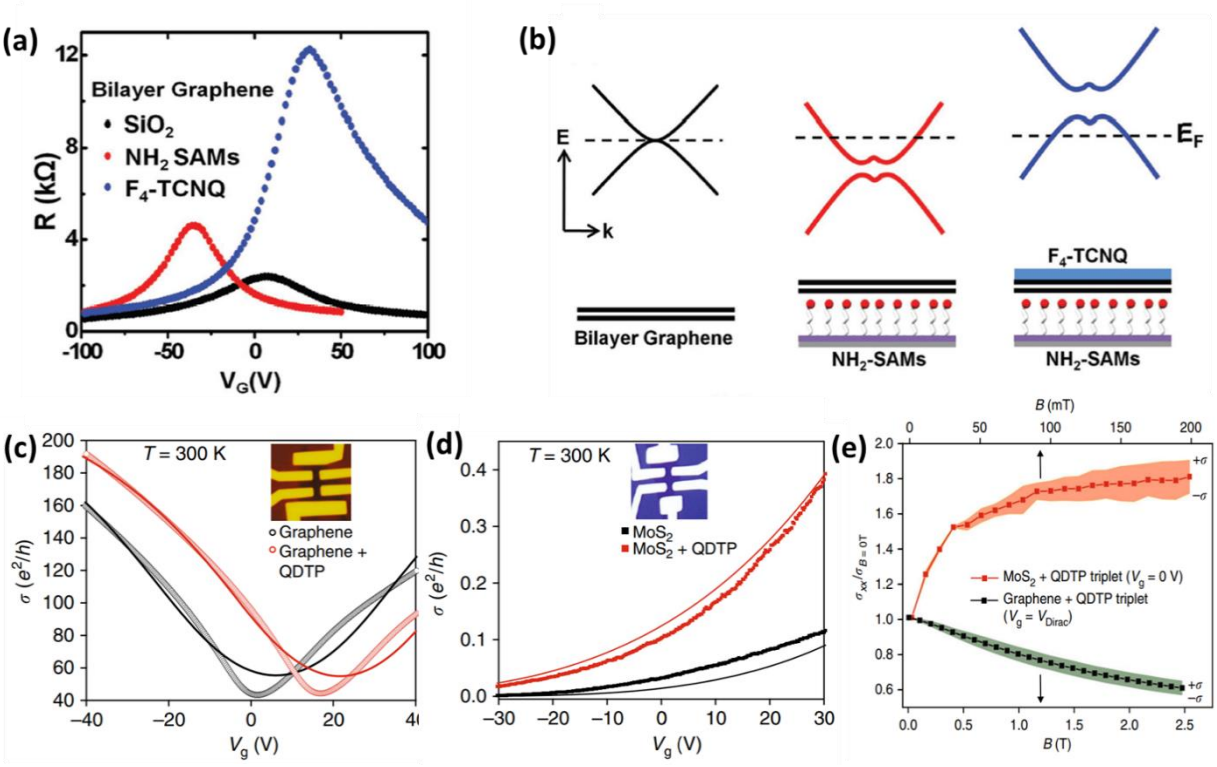


Figure 1.17. *(a) R-Vg characteristics of a Graphene decorated with F4-TCNQ molecule. (b) Graphical representation of opening of band gap in bilayer graphene due to dual layer molecule decoration. (c),(d) Transfer characteristics of graphene and MoS_2 FET decorated with QDTP molecule, shows a significant effect of doping in 2D materials.(d) magneto conductance of QTDP decorated graphene and MoS_2 behaves differently with magnetic field. (a,b) are taken from the reference [95],(c,d,e)are taken from reference [101].*

However, the reversibility poses a challenge in envisioning a stably doped graphene, as the adsorbed gaseous species can be easily desorbed. In addition to adsorbed gases, simple molecular

derivatives with electron-withdrawing or donating functional groups have been introduced to graphene, resulting in p- or n-doping. This diversified approach provides further avenues for tailoring the electronic properties of graphene, paving the way for enhanced versatility in electronic applications.

Theoretical and experimental studies have shown that decorating graphene with molecule can induce a small band gap into the graphene. The perpendicular electric field applied by the molecules to the bilayer graphene system breaks the inversion symmetry in graphene leading to opening of band gap in graphene[95].

By integrating graphene with photosensitive semiconducting nanoparticles or nanosheets, several research groups have showcased the development of highly sensitive phototransistors[96–100]. These devices exhibit both high carrier mobility and exceptional gate control, effectively enhancing the detectivity across a spectrum of light wavelengths. This innovative approach combines the inherent high mobility of graphene with the photosensitive properties inherent in semiconducting molecules.

The study of graphene decorated with magnetic molecules has unveiled a fascinating realm of material properties, offering a convergence of exceptional characteristics from both graphene and the magnetic entities. Researchers have extensively investigated the resulting hybrid materials to discern their unique features and potential applications. The introduction of magnetic molecules onto the graphene lattice imparts intriguing magnetic properties to the material, opening avenues for spintronic applications[101,102]. The interaction between the magnetic moments of the molecules and the electronic state in graphene leads to tunable magnetic behavior. Moreover, the decorated graphene systems often exhibit enhanced electronic transport properties and spin-polarized currents, making them promising candidates for spin-based devices. The synergistic effects arising from the combination of graphene's outstanding electrical conductivity and the magnetic functionalities of the molecules provide a rich platform for advancing the field of graphene-based materials with tailored magnetic properties.

1.7 Motivation of the thesis

2D materials show unique properties when they are exfoliated down to their monolayer or few layer limit. In principle, graphene was anticipated to manifest ballistic transport phenomena,

particularly under conditions of reduced temperatures where the phonon contribution is minimized. However, in reality, the transport characteristics of graphene were found to align more closely with the diffusive behavior rather than ballistic, conforming to semi-classical Boltzmann transport equations. Studies on 2D semiconductors, including MoS_2 and WS_2, have shown empirically that their mobility differs substantially from what theoretical models would have predicted. In the context of graphene on SiO_2, the electron mobility is constrained to 40,000 $cm^2V^{-1}\ s^{-1}$ due to the scattering of electrons by optical phonons originating from the substrate and the generation of electron-hole puddles[69]. Notably, upon substrate removal, the mobility of graphene has experienced a significant increase by several orders of magnitude. It has also been observed that the presence of high-k dielectric like Al_2O_3, HfO_2 can enhance the mobility of the device significantly. All these experimental and theoretical observation indicate towards the role of substrate induced and intrinsic defects in the transport characteristics of these two-dimensional materials. This prompted us to investigate the characteristics and effect of these disorder in the transport properties of these 2D materials, which is equally important for fundamental and application point of view.

In this thesis, we have primarily concentrated on the temperature dependent conductivity and low frequency measurement of these 2D devices. Typical time-averaged transport measurements, such conductance or resistance, are not sufficient to explain the effect of dynamic disorder in these devices. Being directly sensitive to the ability of an electronic device to screen external potential fluctuations, the low frequency noise in electrical transport has been shown to reflect the scattering mechanisms due to the mobile defects involved in the electrical transport. Similar to carbon nanotube field effect devices, it was found that the noise in graphene FETs was primarily caused by fluctuating charge traps within the SiO_2 substrate. Furthermore, it was observed that the noise behavior with gate electric field is different for SLG and BLG. This difference was ascribed to the difference in the electronic structure and the field-induced gap formation in the case of BLG. Following this there are several works in understanding the charge noise in graphene transistors, however, some aspects of the substrate on the noise in this graphene FETs are not known to the community. Hence, in this thesis, first we aim to study the effect of lightly doped Si/SiO_2 substrate on the electrical transport and noise mechanism in graphene FETs, important for possible futuristic high frequency applications and has not been addressed earlier. Then we focus on understanding the charge transport and noise in a relatively new 2D semiconductor, tellurene. Tellurene has been

successfully synthesized using hydrothermal method and the initial measurements in its field effect geometry exhibits high mobility with p-type transfer characteristics. Since there are very few 2D semiconductors available with p-type characteristics, telluerene is no doubt a promising material to explore. More importantly, its environmental stability makes it perfect material for technological applications. Here, we first aim to synthesize tellurene and fabricate FETs and characterize its transport behavior. The focus will be to address the charge noise behavior and its possible mechanism through temperature dependent transport and noise measurements.

Finally, we would like to address another important aspect in the field. Since 2D materials possess a large surface area, there is a possibility to modify their intrinsic behavior by grafting foreign elements. There are multiple attempts to introduce functionalities in to this 2D materials, either by mixing and aligning these 2D materials on top of each other or by decorating it with functional molecules or semiconducting quantum dots. With this goal, we focus on functionalizing graphene using organometallic spin crossover (SCO) nanoparticle, which can change its spin state by the application of external stimuli like pressure or temperature. The aim will be to synthesize and characterize such hybrid materials and create tunable functional devices, sensitive to the spin transitions.

1.8 Organization of the thesis

Chapter 1 introduces to the field of 2D materials (like Grapene and 2D semiconductors) describing their basic properties like crystal structure, band structure, and their electronic properties. It also introduces to the scattering mechanism and the sources of scatterers which effects the electronic transport properties in these 2D materials. Previous studies show that the substrate and the defects in the lattice of the 2D materials play an important role in the electronic transport properties. This chapter also introduces to the basic understanding of 1/f noise spectroscopy. It also introduces to functionalization of these 2D materials to make hybrid functional devices.

In **Chapter 2,** we describe the various experimental methods and techniques employed to carry out the measurements. We commence the chapter with an elaboration on the mechanical and chemical exfoliation of 2D materials and characterization techniques. After that, we describe the

process of fabricating the device, which involves electrode patterning and metal deposition. Finally we elaborate various transport and noise measurement procedure in detail.

In **Chapter 3**, we report how the substrate plays a crucial role in determining the transport and low-frequency noise behavior of graphene field-effect devices. Here, we present the electrical transport and low-frequency noise measurement in CVD grown Graphene field effect transistor fabricated on a lightly doped (p+ doping ~ $10^{15}/cm^2$) Si/SiO_2 substrate. Our systematic characterization of transport, noise, and capacitance at various temperatures reveals that the remote Si/SiO_2 interface significantly influences charge transport in graphene, enabling the sensing of charge fluctuations within the bulk of the silicon substrate by the graphene channel. We show that graphene transport is severely affected by the formation of depletion, inversion and accumulation region at the remote substrate/oxide interface, establishing the role of substrate doping.

In **Chapter 4,** to overcome the limitation of graphene because its zero-band gap, we endeavored to functionalize Graphene and its derivative (rGO) with a spin crossover (SCO) molecule capable of altering its spin state under external perturbation. We observe that the spin-crossover behavior is affected by the presence of graphene. A detailed characterization proves that the charge transfer between graphene and SCO molecule can alter the spin transition temperature and magnetic behavior. We also show that the SCO behavior can be observed in the hybrid electronic devices.

In **Chapter 5,** we try to understand the electronic transport in a low-band gap semiconductor Tellurene. By synthesizing few-layer Tellurene using hydrothermal method we fabricated field effect devices and characterized them through temperature dependent transport measurements. We also provide a systematic low frequency measurements and try to understand its origin from the analysis of the data.

In **Chapter 6,** we provide a concise conclusion to the present thesis, offering insights into its limitations and outlining potential avenues for future research to address these shortcomings.

Chapter 2

Experimental techniques

In this chapter, we provide a concise introduction to the experimental techniques employed in this thesis. The first section encompasses information on device fabrication. The second section will cover a description of the cryostats, which are essential for measuring the devices at low temperatures. Moving on to the third section, we describe key transport measurement techniques utilized in this study, namely, conductance measurements and electrical noise.

2.1 Device fabrication

2.1.1 Preparation of 2D flakes

- **Hydrothermal Exfoliation**: Hydrothermal synthesis, one of the most widely employed techniques for fabricating nanomaterials, is fundamentally a solution-driven chemical reaction process. Within a hermetically sealed vessel, the chemical reactions unfold as the solution is elevated above ambient temperature and subjected to a pressure surpassing that of the atmosphere. This controlled environment fosters the growth of crystals, a crucial step in nanomaterial production. The apparatus facilitating this process comprises of two integral components: a robust steel pressure vessel, commonly referred to as an autoclave, and a nestled Teflon chamber ensconced within the autoclave. The autoclave itself is a formidable steel cylinder, engineered with substantial wall thickness to endure the rigors of high temperatures and pressures sustained over prolonged durations. Importantly, the autoclave necessitates inert solvents for optimal performance. A pivotal element of the autoclave system is the closer, which plays a vital role in the controlled introduction of precursor substances. These precursors, already dissolved in solution, are meticulously poured into the Teflon chamber, ensuring they do not exceed 70% of the available space to maintain an efficient reaction environment. The operational sequence follows a precise protocol: first, the autoclave system is heated to a specific temperature, then allowed to gradually return to room temperature post-heating. Finally, the resulting nanomaterial is carefully stored at the base of the Teflon

chamber, ready for further applications and analyses. This intricate process underscores the importance of meticulous control and precision in hydrothermal synthesis.

After the hydrothermal synthesis, the resulting product contains the prepared 2D flakes. These flakes are subsequently cleaned using De-Ionized (DI) water through a centrifugation technique. Following this purification process, the cleaned 2D flakes are dispersed into either in isopropyl alcohol (IPA) or Ethanol solution. They are then transferred onto the target substrate for further characterization and subsequent device fabrication, accomplished through the method of drop-casting.

- **Mechanical exfoliation**: One of the most widely used and straightforward techniques for generating high-quality 2D crystals is mechanical exfoliation. While CVD-based fabrication of 2D materials such as MoS_2, WSe_2, and Graphene can produce samples over large areas, their lower mobility, presence of defects and grain boundaries limit their application in FET. As these materials are stacked by the weak van der Waals force, the layers can be easily

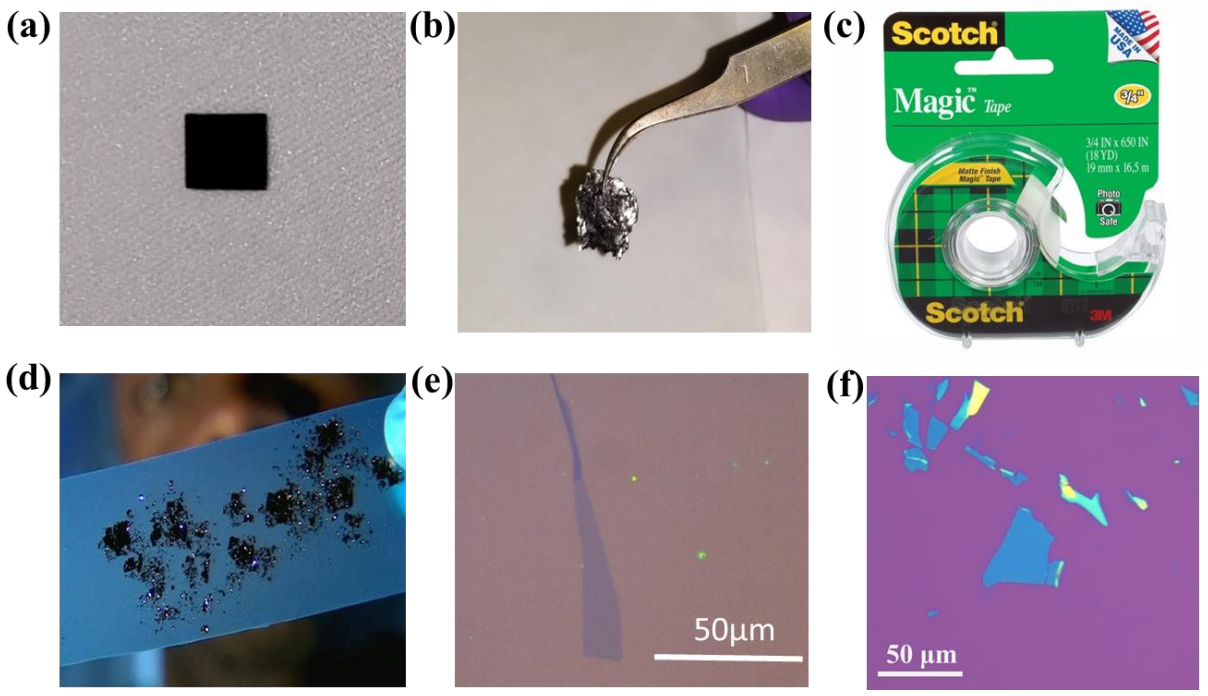


Figure 2.2. *(a) Clean Si/SiO_2 wafer. (b) Single crystal of van der waal's materials (like Graphene, hBN, MoS_2). (c) Scotch tape or the magic tape for mechanical exfoliation. (d) Thin layer of flakes on a Scotch tape cleaved from the van der waal's single crystal. (e) And (f) microscopic image of the exfoliated flakes of Graphene and hBN on Si/SiO_2 wafer.*

separated from the bulk crystal with little force. This process, known as mechanical exfoliation,

is uncomplicated and involves peeling off thin 2D layers from bulk crystals using scotch tape or a similar adhesive tape[1]. In exfoliation processes, a common substrate is Si^{++}/SiO_2, where physical contact is made with the bulk substance. The van der Waals attraction between SiO_2 and various materials allows some of the bulk material to attach to SiO_2 in the form of small flakes. These flakes typically range in size from a few micrometers to several tens of micrometers, and their dimensions can vary significantly depending on the roughness, composition, and other characteristics of the substrate. To produce larger and higher-quality flakes, polished $_{SiO2}$ can be treated with an RCA solution ($NH_4OH:H_2O_2:H_2O$=1:1:5) or exposed to O_2 plasma to increase the surface roughness. We observed that treating the substrate with O_2 plasma cleaning one can get single layer Graphene flakes with dimension larger than 40x40μm. The step of the mechanical exfoliation is described in **Figure 2.1**

2.1.2 Fabrication of van der Waals Heterostructure using dry transfer setup

Heterostructures composed of diverse van der Waals layered materials exhibit exceptionally intriguing electronic and opto-electronic properties. The crucial objective lies in arranging these thin (from single layer to few layers in thickness) layered materials in any desired sequence. While these layers maintain stability on a substrate, they remain adhered thanks to the van der Waals force. However, they are incapable of free standing and are susceptible to mechanical harm, such as tearing or folding, due to factors like thermodynamic instability and stress. By utilizing the support of flexible substrates, these flakes can be successfully relocated without incurring any damage. The attachment of the different layers of the 2D materials is accompanied by Van der Waals attraction. The setup and the stacking process are described in detail below.

2.1.2.1 Mechanical micromanipulator

Here we have designed and customized two heterostructure fabrication setup one using high resolution commercial optical microscope (Model BX53, Olympus) and another with a customized microscope with a zoom lens (Navitar). **Figure 2.2a-b** show the images of the two set up, respectively and the schematic is shown in **Figure 2.3**. The overall heterostructure consist of

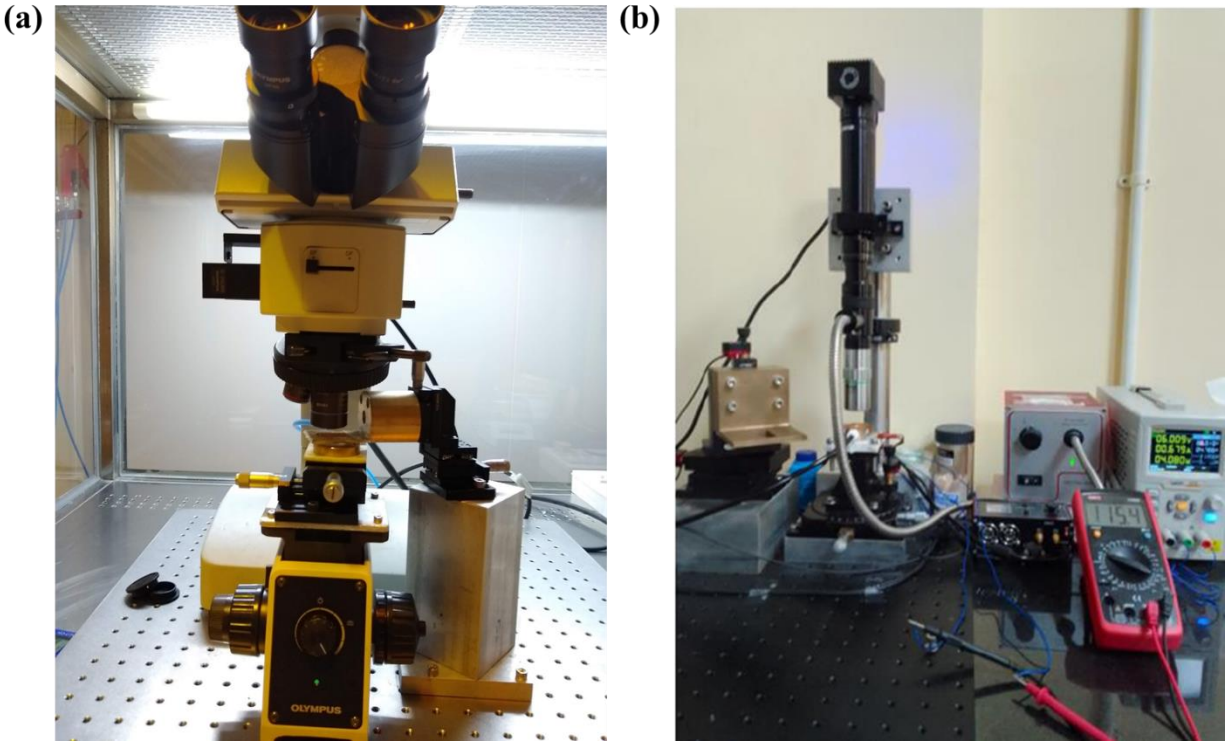


Figure 2.2. *Image of the two dry transfer setup developed in our lab.*

micromanipulation stages apart from the microscope to align the flakes at our desire. The transfer module consists of a sample holder stage and a mask holder stage. Utilizing the XYZ micro controlling system, we initially align two desired samples vertically, namely sample 1 and sample 2. The XY stages provide a precision of 1 μm, facilitating the alignment of materials in the vertical direction. The Z stages play a crucial role in transferring materials for fabricating heterostructures. On the X1Y1 stage, we mount the sample holder and implement heating arrangements for sample 1. We measure the stage's temperature using a pt-100 resistance thermometer. At the sample holder stage, we connect a diaphragm pump to the vacuum port, allowing for straightforward vacuum-and-hold mounting of the lower substrate. To prevent heat conduction to the lower XY stage, we employ Teflon heat isolation. Teflon's substantial thermal expansion/contraction coefficient contributes to achieving exceptional precision in gradually cooling the lower stage. Consequently, we achieve precise control over the stable temperature. The second part of the setup comprises a metal mask holder made of brass and an aluminum stage serving as the base for an identical XYZ stage (X2, Y2, Z2). The mask holder features a window and, due to the step height, can accommodate the mask, which contains sample 2, attached at its bottom.

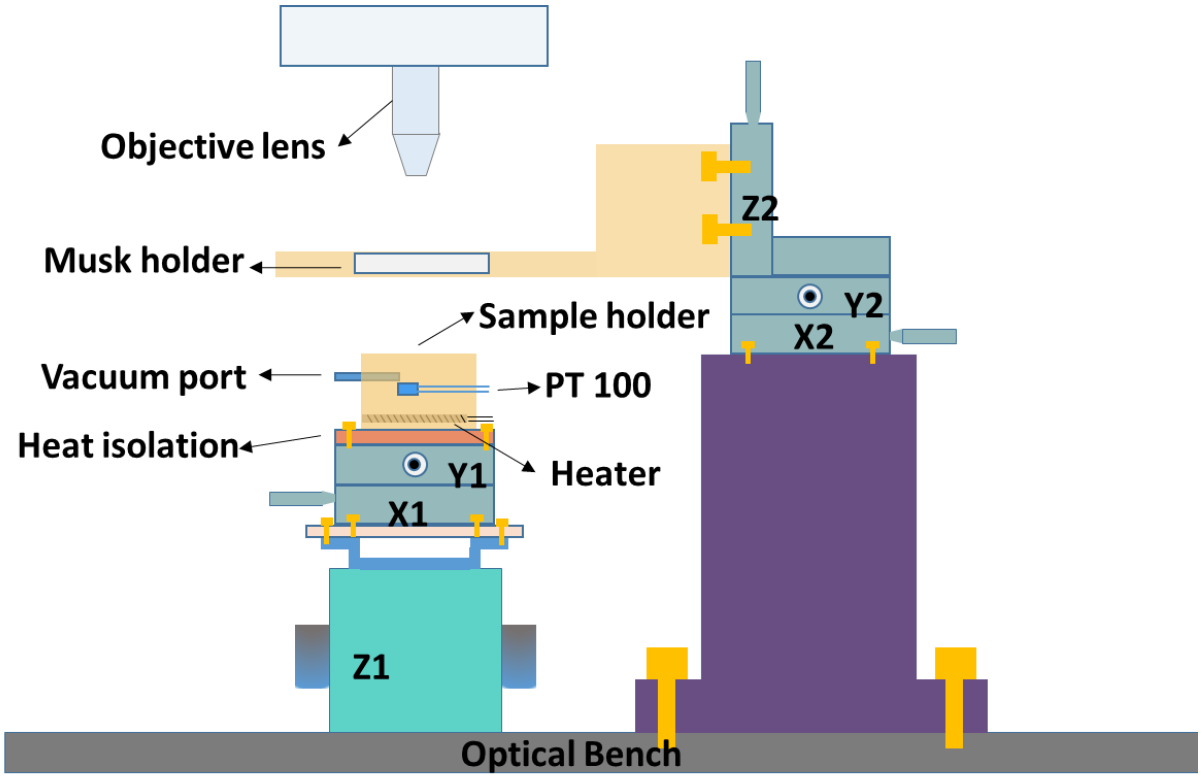


Figure 2.3. *Schematic of the heterostructure fabrication setup, showing the different components.*

2.1.2.2 Preparation of flexible and transparent mask

The process begins with the creation of a flexible mask, achieved by fabricating a custom-made substrate equipped with a sacrificial layer. This layer plays a crucial role in providing essential support for stacking flakes during the transfer process. The substrate itself is composed of a transparent cover glass, approximately 0.5 mm thick, featuring a spherical cap. The spherical shape serves a vital purpose by minimizing points of contact during pickup, ensuring that only the desired flakes are collected while avoiding undesirable regions. Transparency stands out as a key characteristic of the substrate, enabling the monitoring of each step using an optical microscope. In this process, a stamp is employed, which incorporates an adhesive sacrificial layer. The viscosity of this layer can be adjusted through temperature regulation. After the final transfer, any residue can be easily removed using a solvent-based process. To craft the flexible spherical cap, a small drop of PDMS is carefully placed at the center of a clean cover glass and then baked at 200°C for 20-30 minutes. Due to the high viscosity and surface tension of the drop, it naturally spreads out over a small area on the glass plane before baking, resulting in the formation of a spherical cap.

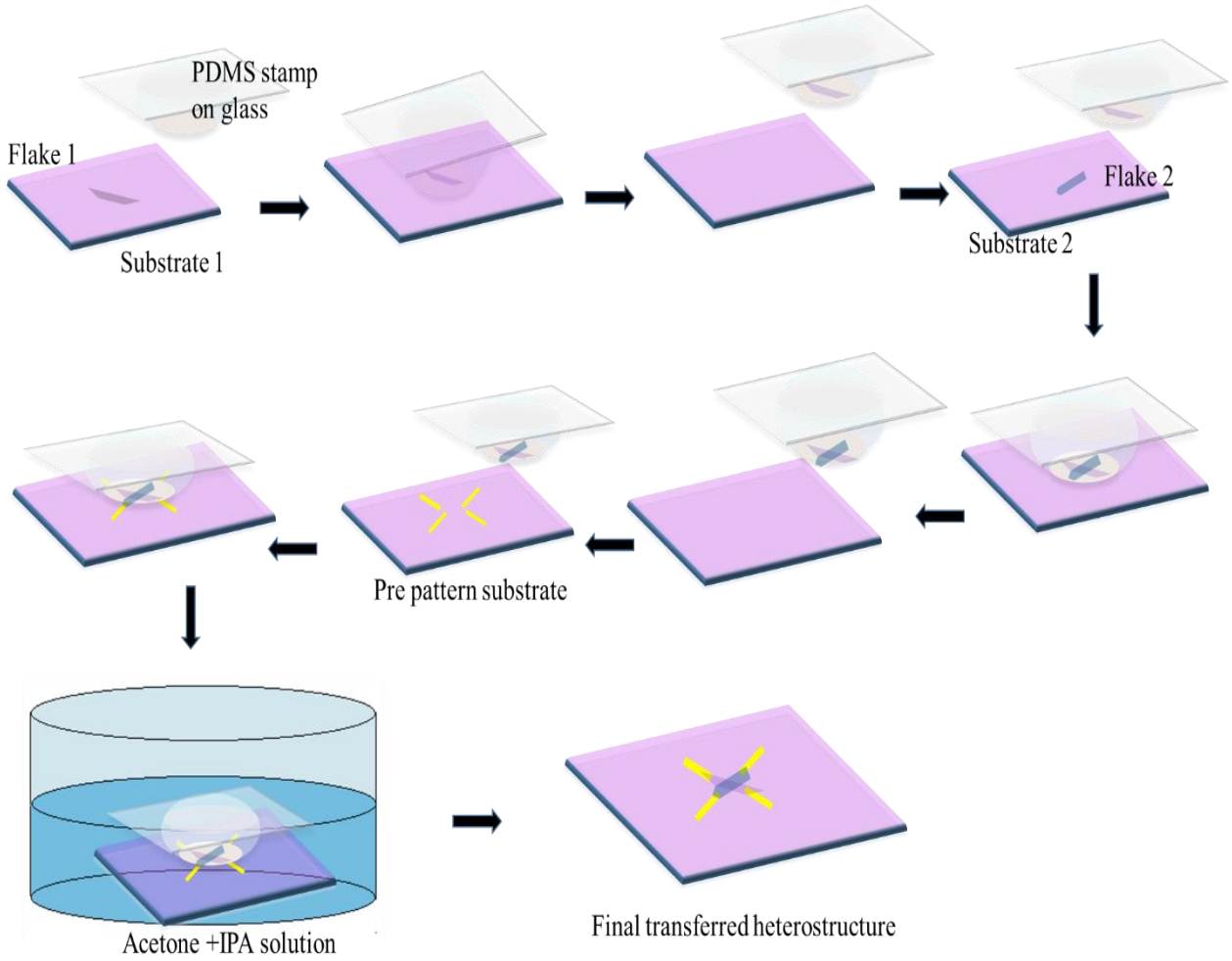


Figure 2.4. *Process flow of the dry transfer process, shown schematically.*

The size of the cap is determined by the volume of the drop, which is meticulously selected to maintain the typical spread dimension within a 1-2 mm diameter circle on the cover glass surface. To enhance adhesivity between the mask and the flakes, a sacrificial layer, known as Lakme color crush (LCC), is applied atop the hemisphere. This layer is spin-coated onto the mask at 8000 rpm and then baked for 2 hours on a hot plate maintained at 90°C, preparing it for the attachment process.

2.1.2.3 Pick-up and transfer process

Figure 2.4 illustrates the step-by-step process for creating the heterostructures. The flexible mask, attached to the metallic holder, is initially positioned downward on the top stage, ensuring proper alignment of the concave surface with the microscope's optical axis. Using the X, Y, and Z stages, the bottom wafer containing the desired flake is carefully moved closer to the stamp, placing the

desired pickup flake at the center. The temperature of the bottom stage is raised to 80° C. Gradually moving the bottom stage in the Z direction, the flake-containing bottom stage makes contact with the LCC-coated stamp. After a brief wait, the LCC separates from the substrate, picking up the flake due to the adhesive force of the LCC being greater than the van der Waals force of the flakes with the substrate. The entire stack is then brought into contact with a pre-patterned SiO_2 wafer, ensuring the flakes are in the desired order. The final transfer is performed at a higher temperature, around 100°-120°C. The vacuum suction is then released, and the substrate is allowed to cool to room temperature. Finally, the stamp and substrate are carefully immersed in a 1:3 acetone-IPA mixture for 3 hours.

2.1.3 Characterization of flakes

2.1.3.1 Optical Microscopy

One cost-effective and efficient way to determine layer numbers is by analyzing the relative

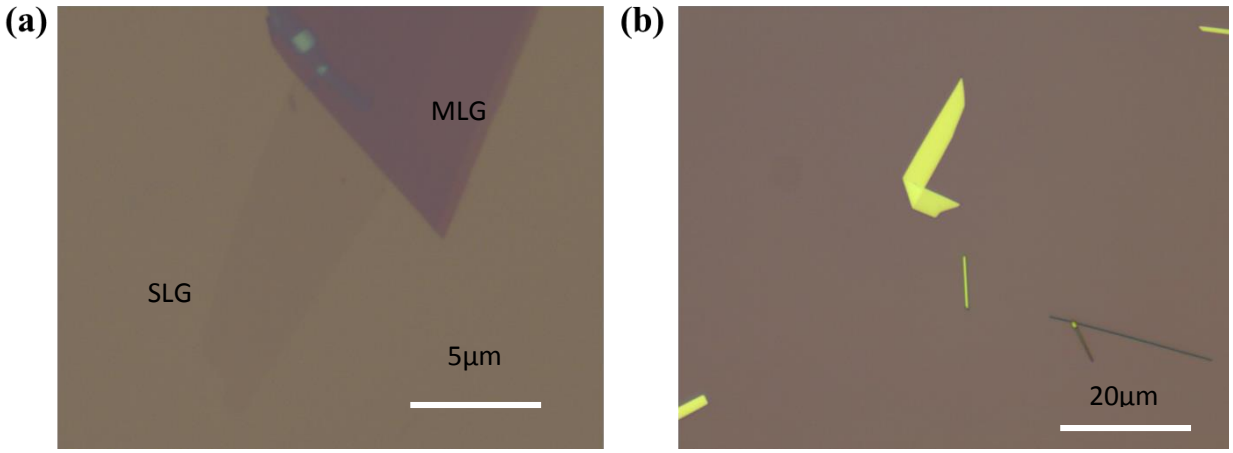


Figure 2.5. *Optical micrographs of (a) Graphene, (b) Tellurene*

intensity difference between the layers and the substrate[103–105] This method hinges on the variation in optical visibility compared to the substrate, which is dependent on the number of layers. When SiO_2 thickness and illumination power remain constant, distinct layer numbers exhibit specific optical colors and contrasts. The interplay of reflected light from SiO_2 and the optical absorption properties of these materials are the key factors determining color and contrast under consistent illumination power. **Figure 2.5** shows the optical micrograph of the different layers of Graphene flakes.

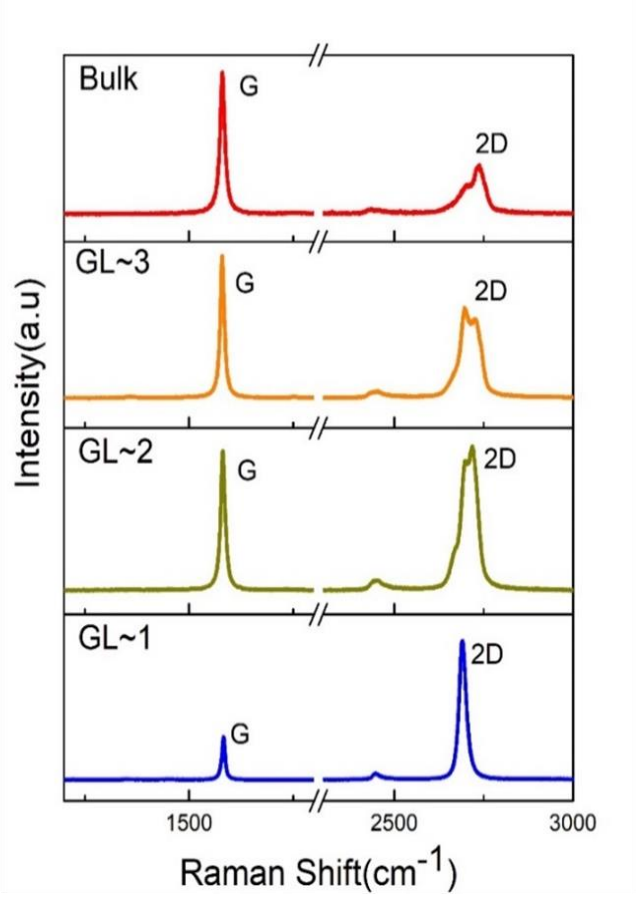


Figure 2.6. *Raman spectra of different layers of Graphene depicting G and 2D peaks*

2.1.3.2 Raman Spectroscopy

Raman spectroscopy stands as a potent, non-invasive, and non-destructive technique for uniquely identifying the type of 2D material and determining its layer number. This method relies on the inelastic scattering of monochromatic light from a laser source, interacting with phonons or other excitations in the sample, resulting in a shift in photon energy. This energy shift provides valuable information about the phonon modes within the system. To carry out this process, a highly monochromatic laser light is directed onto the sample using an optical setup similar to that of an optical microscope. The scattered light is collected and directed through a monochromator and a sensitive detector like a CCD device. The Raman-scattered photons, which share the same wavelength as the incident photons, are typically filtered out using a notch filter. Each of the 2D materials has their unique vibrational spectra and these spectra has a variation in intensity or in position with respect to the thickness of the materials. For example, Graphene has its

characteristics peaks at ~ 1583 cm^{-1} (G peak), ~ 2680 cm^{-1} (2D peak) and ~1350 cm^{-1} (D peak), whereas, Tellurene (multilayer) exhibits peaks around 92 cm^{-1} (E_1-TO mode), 121 cm^{-1} (A_1 mode) and at 141 cm^{-1} (E_2 mode). The details of the origin of the peaks are given in chapter 1. Figure 2.6 depicts the layer dependent Raman spectra of Graphene.

2.1.3.3 Atomic Force Microscopy (AFM)

Atomic Force Microscopy (AFM) is a powerful tool for characterizing 2D materials at the nanoscale. Unlike conventional optical microscopy, AFM operates by scanning a sharp tip over

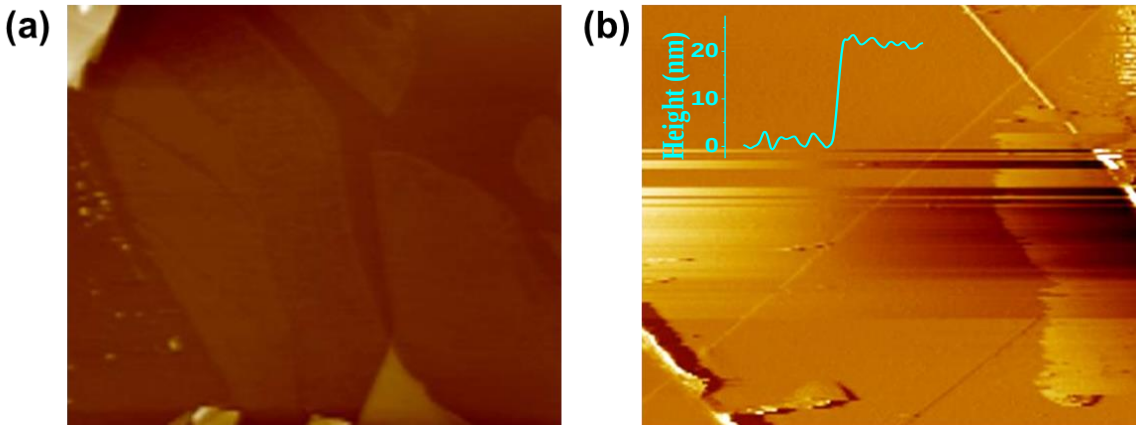


Figure 2.7. *(a) AFM images of exfoliated Graphene showing different thickness (b) AFM image of a Tellurene*

the surface of the material, measuring the interaction forces between the tip and the sample. This allows for high-resolution imaging and precise topographical mapping of the 2D material's surface. AFM operates on the principle of detecting minute forces, as small as 10^{-14} N, between the tip and sample. When the AFM cantilever, carrying the tip, approaches within a few angstroms of the sample's surface, repulsive van der Waals forces between the atoms on the tip and those on the sample induce deflection in the cantilever. The degree of deflection is contingent on the distance (d) between the tip and sample. We have used the AFM to measure the height of the sample, a relative height measurement of the sample gives the information about the approximate number of layers of 2D material present in it.

2.1.3.4 Scanning Electron Microscopy (SEM)

In the SEM instrument, an electron beam is generated from an electron gun through either thermionic emission or cold field emission. Thermionic emission involves electrically heating the

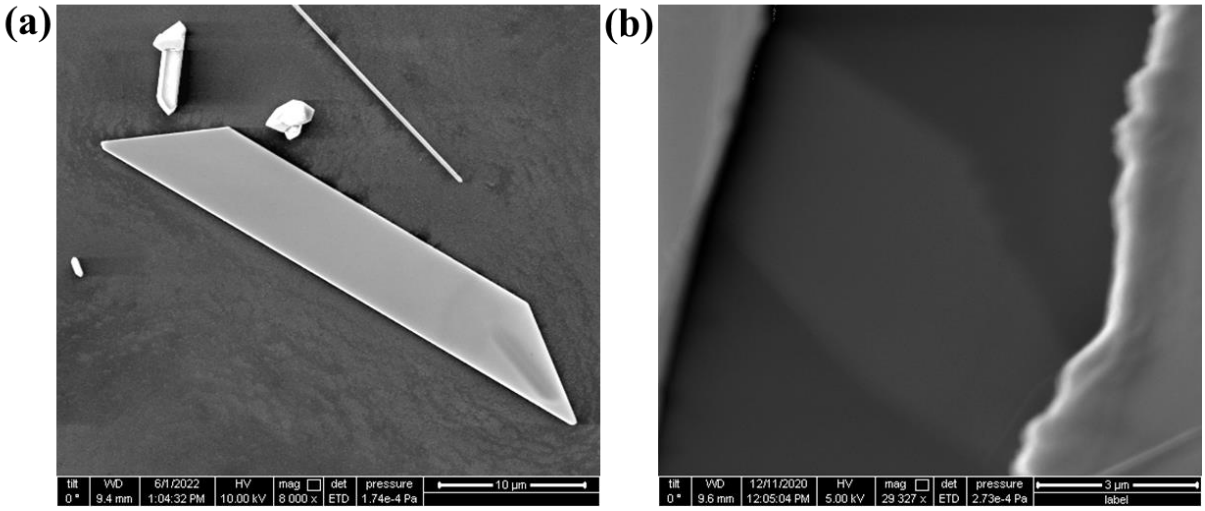


Figure 2.8. *SEM image of (a) Tellurene (b) Graphene*

fine tip of materials like tungsten filament, LaB6 crystal, or ZrO/W (Schottky emitter) to produce electrons. These emitted electrons initially have low energy and need to be accelerated before entering the electron column. This is achieved by applying a high voltage between the electron source (cathode) and the anode plate, creating an electrostatic field that guides and accelerates the electrons. Cold field emission, occurring at room temperature, involves electrons being emitted from the tungsten tip. This method offers advantages like high electron yield and low chromatic aberration, making it suitable for atomic resolution imaging. To prevent burning or oxidation of the filament, a high vacuum (10^{-7} to 10^{-10} mbar) is maintained inside the SEM. Next, an electromagnetic lens composed of insulated copper wire windings, a soft iron cast, and a pole piece is employed to focus and steer the accelerated electron beam. By passing an electrical current through the copper winding, an induced magnetic field is created, guided by the lens' pole pieces. This magnetic field deflects the accelerated electrons, causing them to follow a circular path through the lenses. To scan the entire surface of a specimen, the search coil and magnetic lenses control the horizontal and vertical deflection of the electron beam. The strength of the magnetic field within the lens can be adjusted to modify the focal width of the beam. SEM operates within a voltage range of 2 kV to 50 kV, with beam diameters varying from 5 nm to a few micrometers. The generated electron beam interacts with the sample surface, leading to the production of secondary electrons, auger electrons, characteristic X-rays, backscattered electrons, and cathode luminescence. Secondary and backscattered electrons are detected and distinguished based on their energy, and SEM images are generated using these two signals through the imaging system. SEM

micrographs offer detailed, three-dimensional insights into the sample surface on a large scale due to the narrow probing electron beam**. Figure 2.8** shows the SEM image of the Tellurene flakes and Graphene.

2.1.3.5 Transmission Electron Microscopy (TEM)

Transmission Electron Microscopy (TEM employs a highly energetic electron beam that passes through the sample, revealing its crystal structure, morphology, and elemental composition. This technique is particularly useful for examining low-dimensional objects, assessing their quantity, size, and shape, as well as identifying features like crystal grain boundaries, structural dislocations. TEM comprising an electron gun generating high-energy electrons, a magnetic condensing lens regulating the electron flow onto the specimen, and other essential components. Positioned

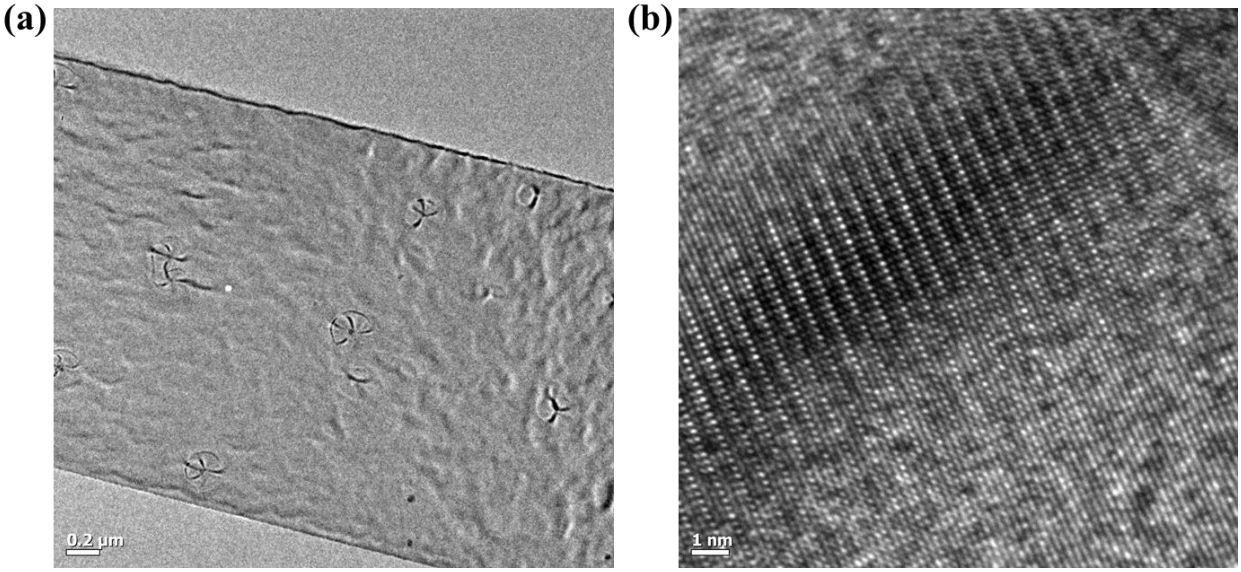


Figure 2.9. *TEM image of Tellurene flakes at different resolution.*

between the objective and condensing lenses is the sample. The magnetic object lens blocks high-angle diffracted beams, while the aperture eliminates the remaining diffracted beams, enhancing image contrast. For higher magnification, a magnetic projector lens is situated above the fluorescent screen. Image capture can be achieved using either a fluorescent screen or a CCD (charged coupled device). When the electron beam interacts with a crystalline sample, many electrons undergo Bragg's scattering across the parallel atomic planes. Depending on the atomic spacing of the crystalline sample, these scattered electrons are gathered using magnetic lenses to generate either a spot or fringe pattern. This pattern provides insights into the sample's atomic

arrangement, phase, crystal plane orientation, and crystallinity. High-Resolution Transmission Electron Microscopy (HRTEM), a form of electron diffraction imaging, enables resolutions up to 0.2 nm, making it highly effective for observing lattice fringes in crystalline specimens. **Figure 2.9** shows the TEM images of a Tellurene flake.

2.1.4 Lithography

Metal contacts on the 2D materials were patterned using either optical lithography or electron beam lithography. In standard optical lithography, a light-sensitive material called photoresist is employed. In the case of positive photoresist, exposure to light causes the exposed areas to degrade, and a developer solution is used to remove the degraded resist, leaving the unexposed areas protected by the optical resist. Following this, the resist is removed from the exposed portion, and

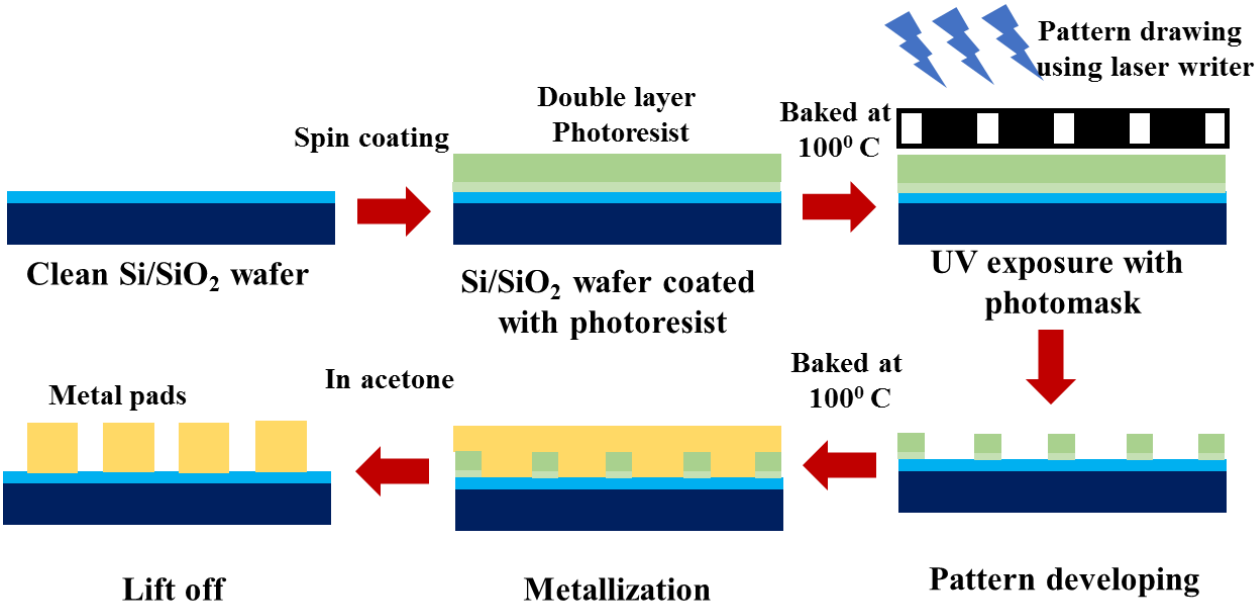


Figure 2.10. *Flow diagram of the process of lithography and metallization.*

desired metal is deposited through e-beam evaporation. Once the metal is deposited, the wafer undergoes a lift-off process, where it is immersed in acetone. This dissolves the unexposed photoresist, leaving behind only the electrical contacts. Achieving a consistently sharp and reproducible lithographic pattern involves employing a bilayer resist coating technique. In this method, the sample is initially coated with a resist that exhibits a high solubility rate in the developer. Subsequently, a second layer of photoresist is applied, characterized by a lower solubility rate in the developer compared to the first resist. During the development process, the

bottom layer undergoes faster dissolution than the top layer, resulting in an undercut, where the top layer overhangs the bottom layer slightly. This bilayer resist strategy enhances the precision and fidelity of the lithographic pattern, ensuring reliable and well-defined features.

The process of fabricating the device and conducting lithography involves several critical steps to ensure optimal results. These steps encompass the meticulous cleaning of the wafer, precise application of resist onto the sample, strategic etching of the sample to achieve the desired pattern, followed by metallization and the crucial lift-off process. Each of these stages contributes significantly to the final outcome of the device. The detailed description of this procedure is outlined below:

1. The wafers with the 2D material were first cleaned with hot acetone and IPA, then blow-dried using nitrogen gas. Following this, they were placed on a hot plate at 120° C to ensure no moisture accumulated on the wafer surface.
2. The cleaned wafer were then spin coated with AZ1512-HS positive photo resist at a revolution speed of 4000 rpm for 60 second. To ensure that all the solvent can evaporate and form a uniform coating, the sample is then baked for a further 1 minutes at 100° C on a hot plate (prebake).
3. The resist coated sample is then mounted in laser writer system where using a 405 nm laser the sample was exposed (with a laser power of 160 mj/cm^2) to give a desire shape to the sample. After developing the pattern in AZ 315 developer for 40 sec we get the sample of our desired shape which then undergoes an etching process.
4. The etching of the lithographic sample was done using plasma etching, in SINTECH ICPRIE plasma etching system. Where for Graphene etching, we have used a low power oxygen plasma with RF power of 6 W for 60 sec. the sample is then dipped into acetone for over an hour to dissolve the excess resist. After dissolving the resist, we get our sample in our desired shape.
5. After etching the sample was first coated with LOR1A as an undercutting resist with a revolution speed of 4000 rpm followed by a baking at 180^0 C, then the second resist AZ1512-HS is coated with revolution speed of 4000 rpm for 60 sec. and again baked for 60 sec at 100^0 C.

6. The desired electrical contacts were then defined using the laser writer with the similar laser power and the pattern were developed for 35 sec in the developer. The sample is then baked at 100^0 C (post bake) for 60 sec and again developed for 45 sec. The second developing helps to create the undercut in the pattern properly.

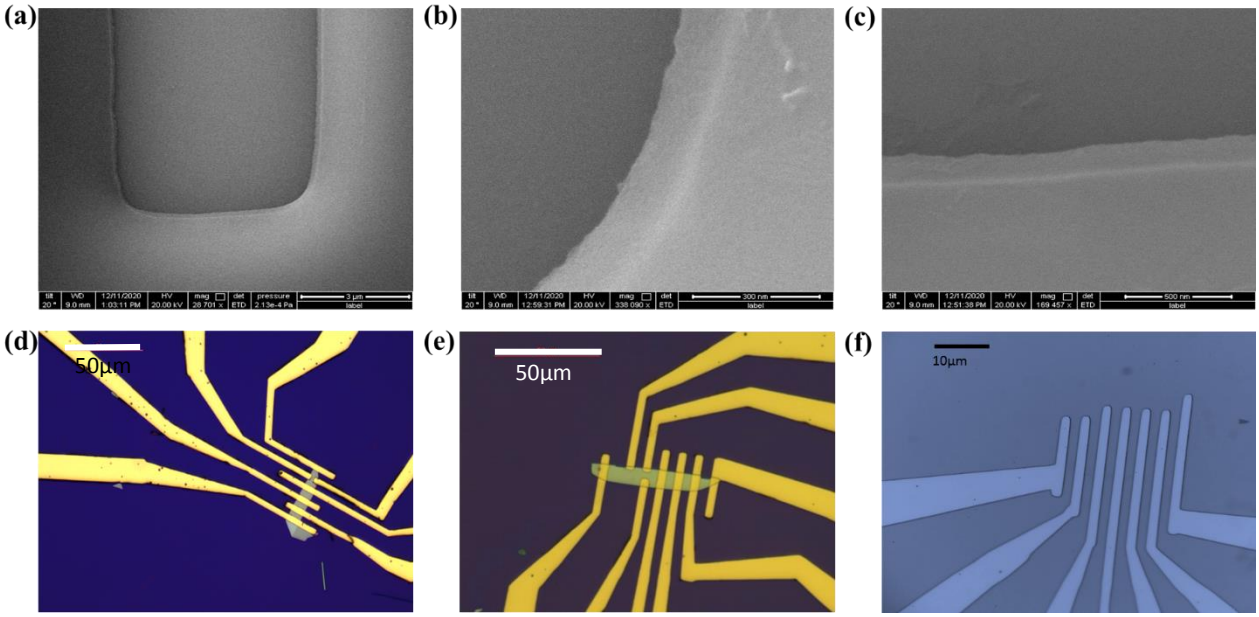


Figure 2.11. *(a), (b), (c) SEM images of the resist profile after the development in developer. (d), (e), (f) Optical micrograph of various devices.*

7. Now the sample were taken for metallization. The metallization were done using e-beam evaporation system, where at high vacuum the metals like Cr/Ti/Au were evaporated at a rate of 0.3 A/s. After deposition of 50-60 nm of metal the sample were taken out for lift-off. The samples are removed after deposition and submerged in acetone for over four hours. Acetone dissolves the photoresist, leaving the deposited metal on the substrate behind. Acetone is injected into the sample using a syringe, aiding in the removal of unwanted Au from the substrate (lift-off). The sample is then blow-dried with a nitrogen gun after being rinsed in IPA.

2.1.5 Bonding of device

The final step in the fabrication process is device packaging. Following thermal evaporation, the sample wafer is affixed onto a ceramic chip carrier. This carrier is equipped with 20 gold pads, which serve as the points of contact for the device contact pads via wire bonding. The gold-coated

base of the chip carrier can function as a global back-gate for the device. Electrical contact between the contact pads of the sample and the contact pads of the chip carrier is established using Au wire bonding. Two types of Au wire bonding were employed: (i) Ball bonding and (ii) direct silver epoxy bonding. Details of the bonding process are provided below:

Ball bonding is utilized to connect the gold pads of the sample to the connecting pads of the chip carrier. This process involves the use of a ceramic capillary tip through which the gold wire is threaded. In the initial stage, a high voltage spark is generated at the tip of the wire, melting it into a spherical shape due to surface tension. The resulting ball tip is then brought into close proximity with the sample's gold pads, and ultrasonic energy is applied to weld the gold ball onto the sample's gold pads. Subsequently, the wire is directed towards the contact pads of the chip carrier, forming a loop and then welded using the same process, without forming a ball.

In an alternative process, the device and chip carrier leads are directly bonded using an Au wire and silver epoxy. After applying a blob of silver epoxy onto the gold pads, the device is cured at 120° C.

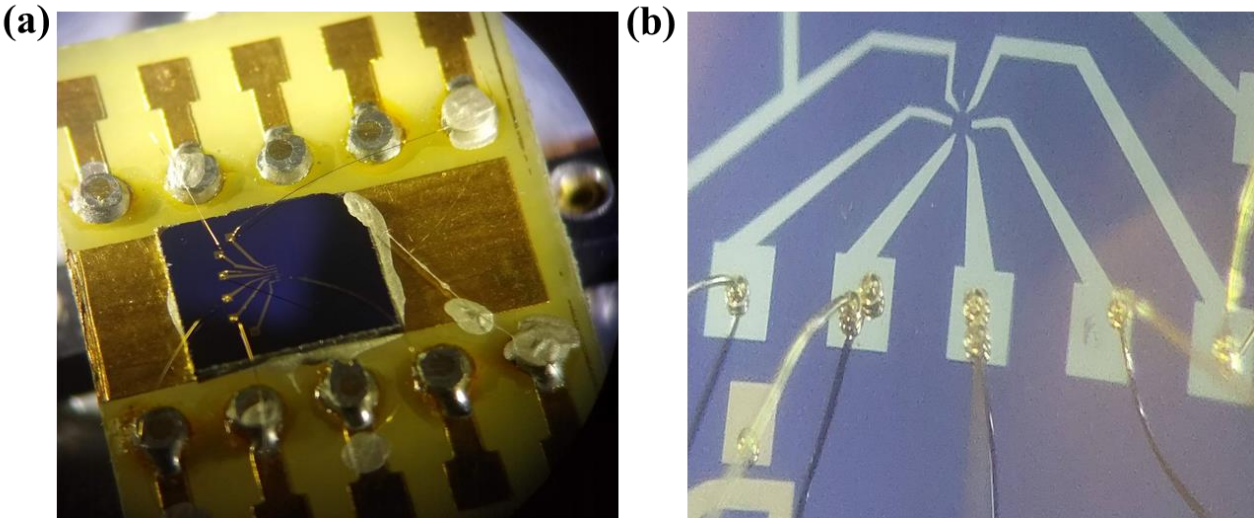


Figure 2.12. *Photographs of the ball bonded device.*

2.2 Low temperature measurement setup

A variable temperature cryostat is an essential tool for conducting electrical transport measurements. To facilitate this, we have meticulously designed a dip stick, the schematic of which is depicted in **Figure 2.13**. This dip stick comprises several key components, including a

sample holder affixed to a copper plate, a primary stainless-steel tube for wire connections, four smaller diameter stainless steel tubes serving dual purposes - accommodating heater wire connections and housing the gas purging pipe, and a vacuum jacket that effectively isolates the main samples from the surrounding liquid nitrogen. It is imperative to create a vacuum within the chamber to ensure a gradual and controlled cooling process for our sample. The dipstick can hold a vacuum level of the order of 10^{-6} mbar.

The dipstick is outfitted with a 25 Ω manganin heater wire, which enables us to precisely regulate the temperature of the sample stage. Additionally, a PT-100 temperature sensor is strategically positioned in close proximity to the sample holder, allowing us to accurately monitor the temperature of the sample. To optimize thermal conductivity, the wires originating from the room temperature source are meticulously wound around the copper stage, as our sample primarily dissipates heat through these wires during the cooling process. The temperature and heater power

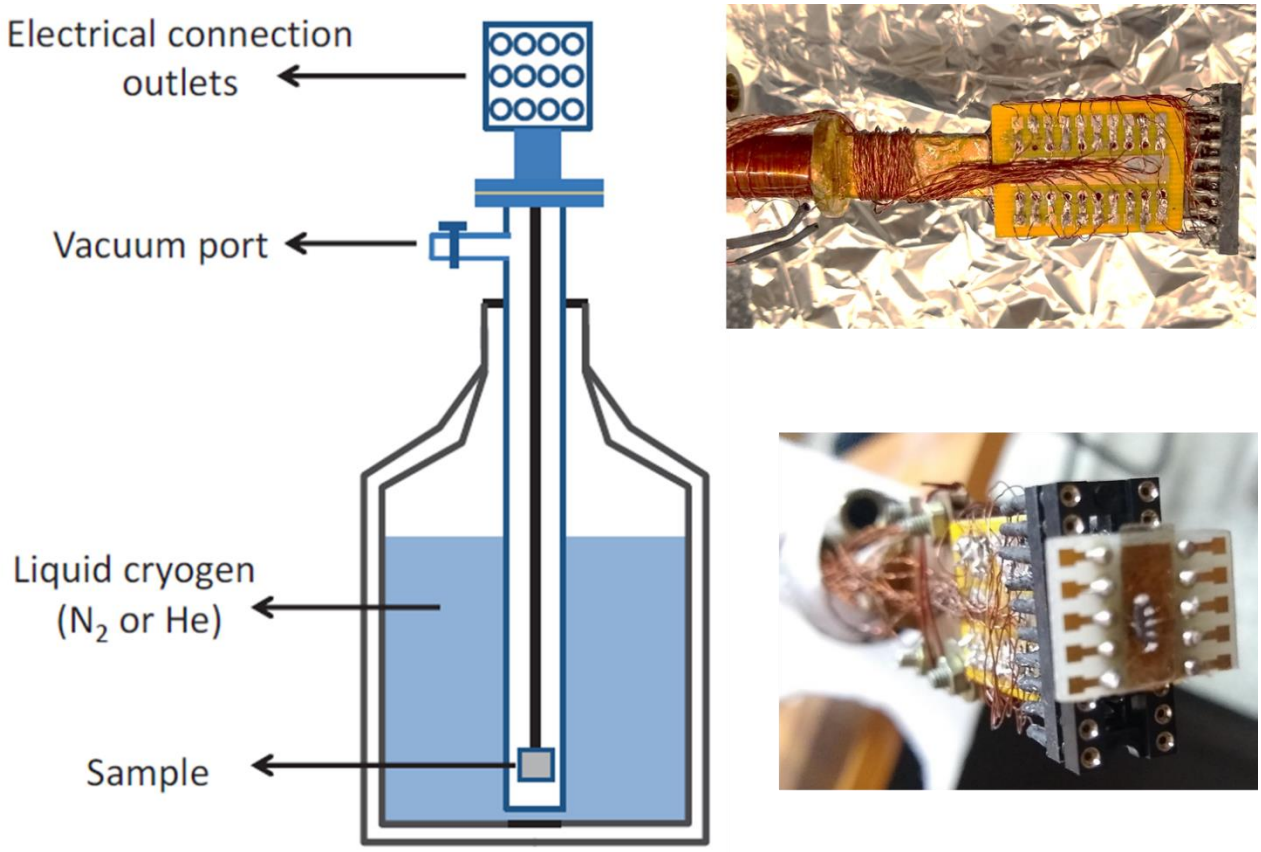


Figure 2.13. *Schematic of the dipstick inside the Nitrogen Dewar (left). Image of the sample holder of the dipstick (right side).*

is controlled by a temperature controller (Lakeshore). The optimized PID of the temperature controller provide a temperature stability in the order of 10^{-3} K at the sample stage.

For connecting the sample wires to the instruments, we employ BNC cables, which are then affixed to a breakout box. To ensure that our sample never remains in a floating state, we implement a three-way switch and establish connections. This configuration ensures that the sample is either grounded or set to the desired voltage level for the experiment.

2.3 Electrical transport measurement techniques

In this section we provide brief description about the various electrical measurement performed in this thesis namely, current-voltage (I-V) measurement, gate dependent resistance measurement (R-Vg), capacitance measurement (C-V), noise measurement.

2.3.1 Two terminal current-voltage (I-V) measurement

The output characteristics of the Field Effect Transistor (FET) serve as a critical means to assess the nature of the sample, whether it displays ohmic or non-ohmic behavior. Linear current-voltage (I-V) characteristics indicate an ohmic response, whereas non-linear I-V characteristics suggest a Schottky-type behavior.

In **Figure 2.14a**, we can observe the setup designed for measuring these I-V characteristics. A Source Measuring Unit (model 2450, Keithley) is employed to apply a source-drain bias (V_{sd}) at one end of the channel, while the opposite end is grounded through a 50Ω terminator. The corresponding current is then accurately measured. Furthermore, SMU is also utilized to assess the DC transfer characteristics of the samples. In this configuration, one source meter is dedicated to measuring the I-V characteristics, while the other source meter is connected to the gate terminal. This comprehensive approach enables us to gain a thorough understanding of the electrical behavior of the sample under varying conditions. It empowers us to distinguish between ohmic and non-ohmic characteristics and even identify any Schottky-type behavior exhibited by the sample.

2.3.2 Four terminal ac resistance measurement

We have performed two terminal and four terminal ac resistance measurement using a lock-in amplifier (MFLI, Zurich instruments). To perform measurements, a low-frequency alternating

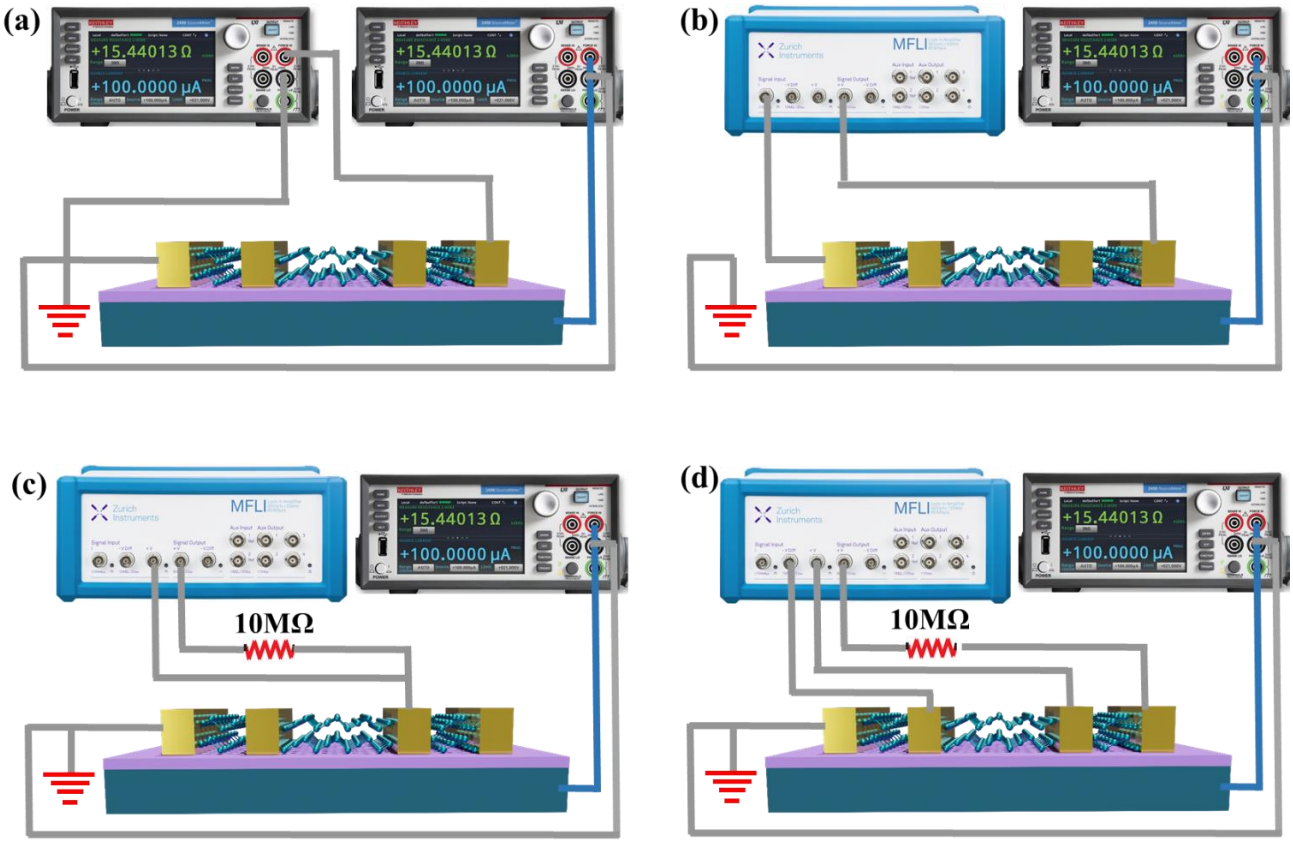


Figure 2.14. *Schematic of various electrical measurement technique (a) 2 terminal d.c. I-V with variation of gate voltage. (b) 2 terminal a.c. conductance measurement with lock-in amplifier in current mode. (c), (d) 2 and 4 terminal a.c. conductance measurement in voltage mode.*

current (ac) bias with a small frequency is applied using a lock-in amplifier. This ac bias is accompanied by a substantial current limiting resistance (R_s), typically on the order of megaohms (MΩ), which is connected in series. And the gate voltage is applied through the silicon global back gate using Keithley 2450 SMU. This arrangement ensures that only a small current (I_{sd}) passes through the device under investigation. The resulting voltage drop across the two voltage probes, denoted as V_{4p}, serves as the basis for calculating the four-probe resistance (R_{4p}), defined as the ratio of V_{4p} to Is ($R_{4p} = V_{4p}/I_{sd}$). It is imperative to maintain a low value for I_{sd} (ensuring that V_{4p} is less than or approximately equal to the product of the thermal energy k_BT and the elementary

charge e) to prevent any undesired heating of the device (D). It is worth noting that the upper limit of resistance that can be accurately measured through this technique is determined by the input impedance of the lock-in amplifier. This limitation arises from the characteristics of the measurement setup and instrumentation used in the experiment.

Two terminal ac conductance is commonly used to measure the high resistance samples (semiconductors). In most cases, a lock-in amplifier is used to supply the bias voltage (V_{ds}) and measure the output current (I_{ds}) at a specific frequency. To detect weak signals and improve signal-to-noise ratio, the drain-source current (I_{ds}) is sometimes amplified by an external current amplifier (Basel) and measured in the A mode of lock-in amplifier. The two terminal and four terminal measurements were shown in **Figure 2.14c, d**.

2.3.3 Capacitance-Voltage (C-V) measurement

Capacitance (C) – Voltage (V) characteristics at different carrier frequencies are often measured to understand the effect of interfacial traps in field effect transistors. We have primarily used an impedance analyzer (MFIA, Zurich instruments) and a low noise DC voltage source (GS200, YOKOGAWA) to measure the CV characteristics in the MOS (Metal-oxide-semiconductor)

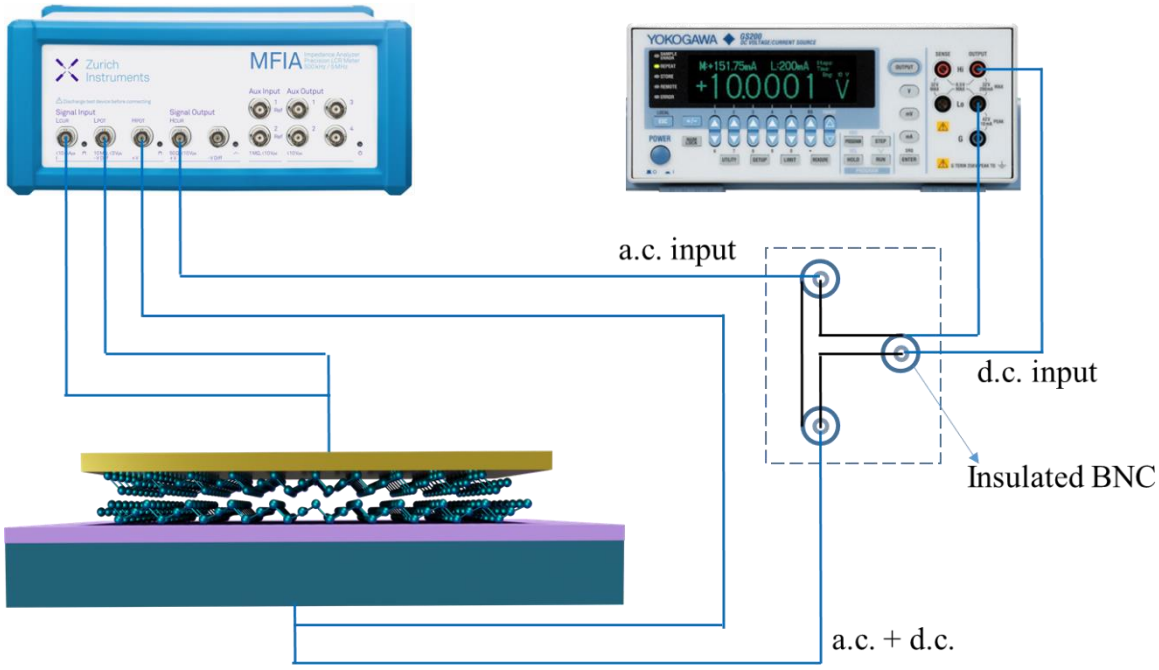


Figure 2.15. *Schematic of the Capacitance vs Gate voltage measurement system using MFIA impedance analyzer and YOKOGAWA source meter.*

structures. To perform the experiment, we have biased the sample through the silicon global back

gate using a variable DC bias voltage mixed with a small ac signal with varying frequency, keeping the sample (2D material grounded) as shown in **Figure 2.15.** At a constant ac bias (finite frequency) we vary the DC bias (gate voltage) and simultaneously measure the capacitance of the system through the impedance analyzer. The CV measurement in our device helps us to understand the variation of capacitance in our system when the system goes through accumulation, depletion, inversion region in the interface of the SiO_2/Si interface.

2.4 Resistance fluctuations or noise measurement

The following section outlines in some detail the framework of resistance noise, a powerful tool for studying the dynamics of charge carriers in a solid-state system. This measurement technique is highly involved, requiring meticulous implementation of electronic circuits and substantial digital signal processing.

2.4.1 Mathematical formulation of Noise

The resistance noise is acquired by measuring fluctuations in voltage at a constant current or fluctuations in current at a constant voltage bias. These fluctuations in voltage drop, denoted as δV, are recorded in memory using a high sampling rate data card. To compute the power spectral density, the first step involves calculating the autocorrelation function, which is defined by the following expression.

$$C(\tau) = \lim_{T\to\infty}\left(\frac{1}{2T}\right)\int_{-T}^{T} dt\ \delta V(t+\tau)\delta V(t) \quad \text{..... (2.1)}$$

The functional form of C(τ) is contingent upon the time scales inherent in the fluctuating quantity, which mirrors the time scales of the underlying physical mechanism. The magnitude of C(τ) at the frequency 1/(2πτ) is determined by a component of the signal at the time scale τ_0. The power spectral density of the fluctuating quantity serves as a measure of the distribution of power in the frequency domain. It is calculated as follows

$$S_V(f) = \int_{-\infty}^{\infty} d\tau\ e^{-i2\pi f\tau}\ C(\tau) \quad \text{..... (2.2)}$$

For a characteristic time scale τ_o, $C(\tau) \propto e^{\tau/\tau_o}$. The corresponding power spectrum is a Lorentzian given by

$$S_V(f) \propto \frac{2\tau_o}{1+(2\pi f\tau_o)^2} \quad \text{..... (2.3)}$$

In a sample there is usually a distribution of time scales, each contributing additively to the noise magnitude. **Figure 2.16a** shows that a few Lorentzian associated with each time scale add up to a dependence that looks like 1/*f* type. This is one way to understand the origin of 1/*f* type of noise.

2.4.2 Measurement scheme

Obtaining accurate measurements of resistance fluctuations in mesoscopic devices is generally challenging due to various factors. This task necessitates the careful elimination of external noises originating from multiple sources, including the measuring equipment, 50 Hz transmission line, and impedance mismatch, as these can easily obscure the device's inherent noise. To achieve dependable noise measurements, it is crucial to implement the measurement scheme and digital signal processing steps while considering these factors.

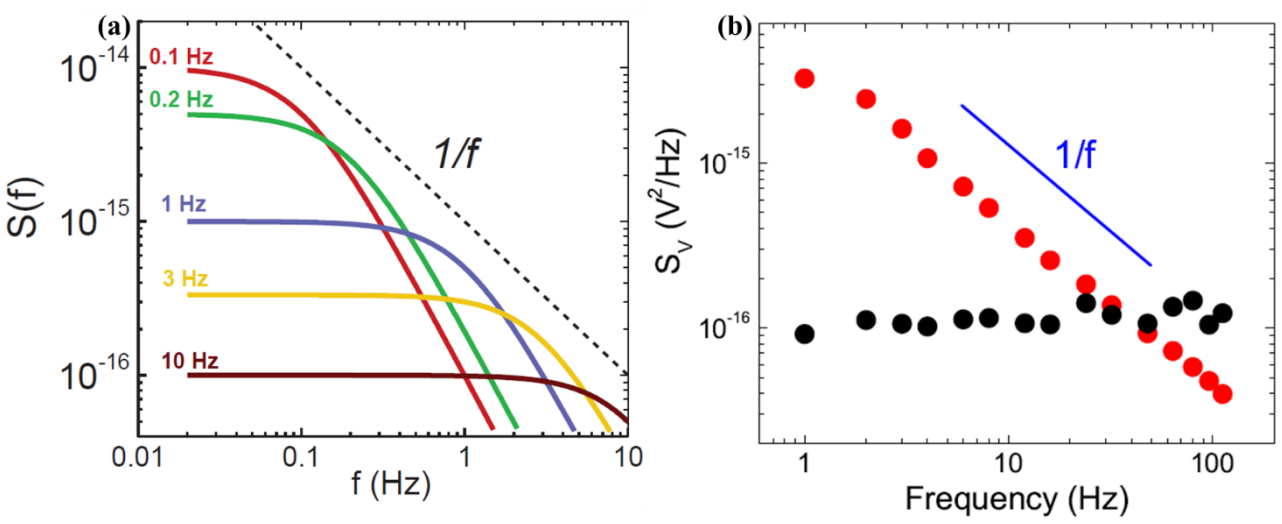


Figure 2.16. *(a) 1/f spectrum in power spectral density is a result of a distribution of several relaxation time scales. (b) Typical 1/f noise spectra recorded from a Graphene device.*

A Dual-channel Lock-in Amplifier (LIA) is utilized, employing the phase-sensitive technique, to measure the fluctuations in voltage drop across the sample. This measurement is carried out while applying an AC current of constant magnitude at frequency f_o. The power spectral density (PSD) of the voltage measurement has two components in it

$$S_V(f) \approx G_0^2[S_V^0(f_o - f) + I_{rms}^2 S_R(f)cos^2\delta] \quad \text{..... (2.4)}$$

The first component, referred to as background noise, primarily arises from voltage fluctuations stemming from Johnson's noise and impedance mismatch. Both of these factors are independent of the excitation voltage. The second component encompasses the 1/f nature noise originating from

the sample, which is directly proportional to the square of the excitation current. In this context, δ represents the phase angle of detection relative to the applied excitation.

For in-plane measurements (when $\delta = 0$), the calculated Power Spectral Density (PSD) comprises both background noise and resistance noise. Conversely, for quadrature measurements ($\delta = \pi/2$), only the PSD from the background noise is evident. The dual-channel lock-in amplifier is capable of performing both in-plane (X component) and quadrature (Y component) measurements simultaneously. This enables the results from these two measurements to be subtracted, yielding the PSD of the resistance noise originating from the sample. This aspect represents a significant advantage of phase-sensitive noise measurement, as it allows for the concurrent measurement and identification of both total noise and background noise**. Figure 2.16b** shows the Y and X-Y components of a noise measurement.

The measurement of noise in resistance or conductance was conducted using the standard circuits for resistance or conductance measurements, as described earlier. The Lock-in Amplifier (LIA) provided continuous signals from its X and Y channels, which were subsequently digitized at a high sampling rate. This digitization process was facilitated by the built-in data acquisition system integrated within the MFLI lock-in amplifier, which was interfaced with LabVIEW programs.

To facilitate efficient data handling, the acquired data was temporarily stored in the integrated memory of the card. Subsequently, it was transferred to the computer's hard disk in segmented intervals. This step ensured that the data was securely preserved and organized for further analysis and processing.

2.4.3 Aliasing elimination and decimation

Data acquisition is a critical aspect of noise measurement, involving the measurement of a fluctuating quantity over time in regular, small intervals with a frequency defined by its inverse, known as the sampling frequency (f_S). However, a challenge arises due to the discretization of signal voltage. Specifically, a signal sampled at frequency f_S cannot distinguish between a sinusoid at frequency f_0 and frequencies of $f_0 \pm kf_S$ for any integer value of k.

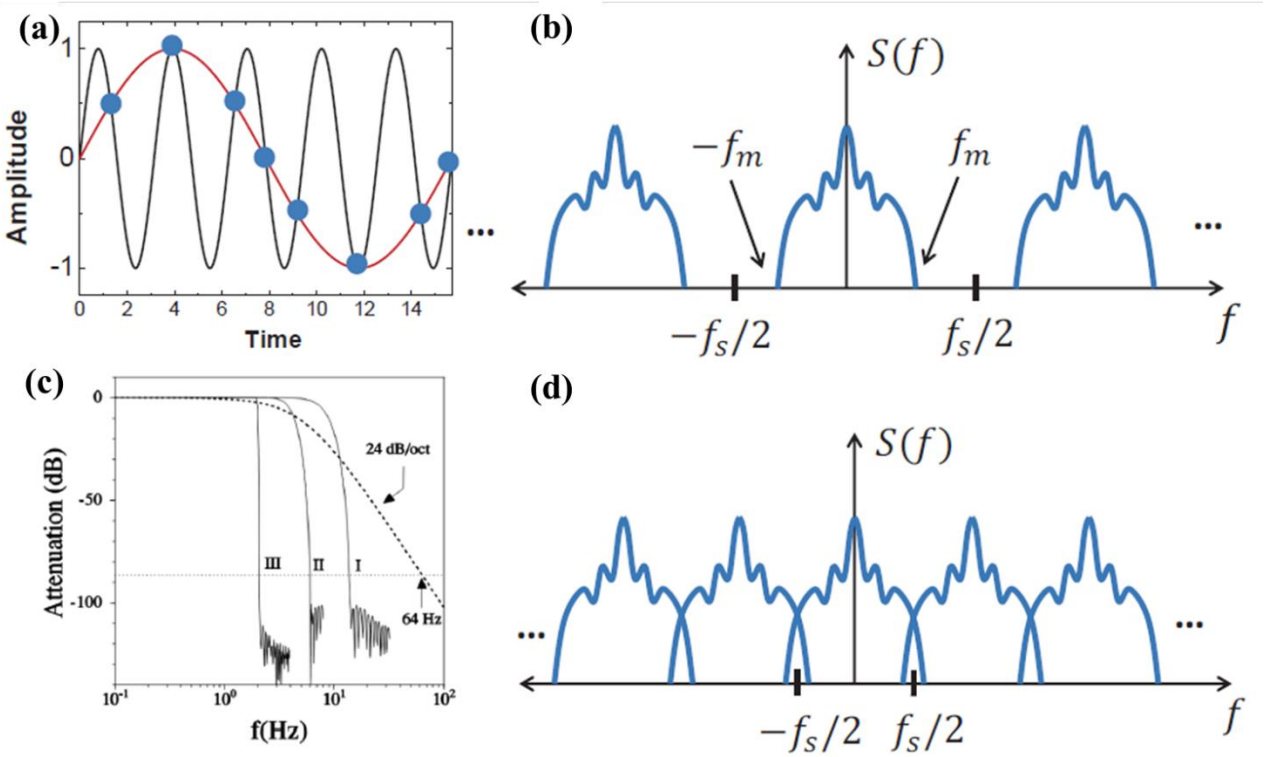


Figure 2.17. *(a) Sampling rate of f_S cannot distinguish between signals of frequency f and $f \pm kf_S$. (b) The spectral width is captured without aliasing when it is contained within the bandwidth f_S. (c) The response function of three-stage digital filter to enable a higher roll-off than the lock-in amplifier's 24 dB/octave (in dashed line) to avoid aliasing. (d) Aliasing occurs when the spectral width is larger than the bandwidth f_S.*

This situation is illustrated in **Figure 2.17a**, where the sampled points of the signal appear to represent one cycle of a sinusoid. In reality, they correspond to a sinusoid with five cycles. This discrepancy arises because the sampling rate is insufficient to capture high frequencies in the signal. Therefore, reliable sampling is contingent upon the absence of high-frequency components in the signal, which can be achieved through the application of appropriate low-pass filters. This scenario is exemplified in **Figure 2.17b**, where the signal contains frequency components up to f_m.

The frequency spectra of the sampled signal produce multiple images or aliases of the real signal, each corresponding to integer values of k and separated by f_S. When f_m is less than half of the sampling frequency ($f_m < f_S/2$), the replicas do not overlap, ensuring that the sampled data is reliable. However, as depicted in **Figure 2.17d**, when f_m exceeds half of the sampling frequency ($f_m > f_S/2$), the replicas overlap. Consequently, the measured signal at a particular frequency may actually contain components from another frequency. This phenomenon is referred to as aliasing.

The criterion for reliable measurements is that f_m should be less than half of the sampling frequency ($f_m < f_s/2$), a principle known as the Nyquist criterion.

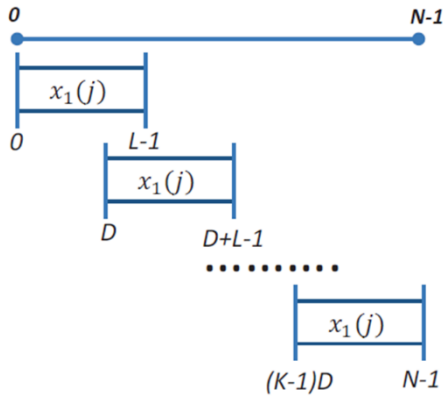
To achieve the desired bandwidth of 10 Hz in our experiments, it is imperative to employ a robust low-pass filter capable of effectively attenuating higher frequencies. Although the lock-in amplifier offers a 24 dB/octave filter, this alone may not suffice to eliminate potential aliasing originating from stronger signals, especially the 50 Hz transmission line. In such cases, higher roll-offs for low-pass filters can be attained through the use of digital filters. This is crucial because at these frequencies, the magnitude of the 1/f noise drops below the background noise level. This process in time domain is known as decimation and the procedure is described as follows:

- For a required bandwidth of $fs/2$ (~ 10 Hz), the signal is sampled at a rate which is f'_S ~64 times that of fs (i.e. f's ~ 1000 Hz), with lockin time constant selected closest to $fs/2$(~10 ms), and the maximum possible roll-off (~24 dB/octave). This cuts off any component beyond $fs/2$ with an attenuation > 105 at $f'_S/2$, which is effective bandwidth before decimation.

- The signal is then passed through a digital anti-aliasing filter having a cut-off at $f'_S/2$, and with an effective roll-off which can be as high as 80-100 dB/octave which effectively removes all traces of any stray signals beyond $f'_S/2$.

- The data is then re-sampled taking every 64th or 128th data point, so as to effectively bring down the sampling rate to fs, without the presence of any aliased signal. Using this technique it was possible to obtain very clean spectra over several orders of magnitude in frequency.

- In order to speed up this process and for optimal memory usages, the decimasation is done in three stages. For a decimation by a total factor of 64, we have used the set of successive decimation factors of 8, 4 and 2. The roll-off which can be obtained from this scheme is up to 100 dB/octave and is plotted in **Figure 2.17c**.



$$x_1(j) = x(j) \qquad j = 0,1,\dots,L-1$$
$$x_2(j) = x(j+D) \qquad j = 0,1,\dots,L-1$$
$$x_K(j) = x(j+(K-1)D) \qquad j = 0,1,\dots,L-1$$

$$w(j) = \frac{1}{2}\left[1 - \frac{\cos 2\pi j}{N}\right] \qquad \text{for } j = 0,1,2 \dots L-1$$

Figure 2.18. *Welch periodogram method used to estimate the power spectral density from the time series data.*

2.4.4 Power Spectral Density calculation

The time series, once decimated according to the aforementioned process, is anticipated to be devoid of any undesirable artifacts, such as aliasing and external noises. This refined data can now be effectively utilized for the calculation of the Power Spectral Density (PSD). The PSD is determined using the Welch method, which involves the averaging of periodograms. The schematic representation of this method can be found in **Figure 2.18**. It involves dividing the complete data set, consisting of N points, into smaller overlapping segments of length L, denoted as the set xi (as depicted in the figure). Subsequently, each of these segments is normalized using the Hanning window function denoted by w(j) (as illustrated in **Figure 2.18**). Finally, fast Fourier transforms are performed, and the power spectrum is computed independently for each segment using the given expression.

$$A_k(n) = \frac{1}{L}\sum_{j=0}^{L-1} x_k(j)w(j)e^{-\frac{2kijn}{L}}, \qquad k = 1,2,\dots K \quad \dots\dots (2.5)$$

$$P_k(f_n) = \frac{L}{U}|A_k(n)|^2 \quad \dots\dots (2.6)$$

$$\text{Where} \quad U = \frac{1}{L}\sum_{j=0}^{L-1} w^2(j) \quad \dots\dots (2.7)$$

Where $f_n = n\left(\frac{2f_{max}}{L}\right)$, for $n = 0, 1, 2, \dots L/2$. The unit of frequency is discrete steps of $2f_{max}/L$ and $f_{max} = f_s/2$ is the effective sampling rate after decimation.

Finally, the power spectral density is calculated by averaging over all periodograms:

$$S(f_n) = \sum_{k=1}^{K} P_k(f_n) \quad \text{for } f \leq f_{max} \text{ ……..…… (2.8)}$$

There is a trade-off in choosing the parameters L and D. Higher L will results in higher resolution of power spectrum but too high would mean lesser number of segments to average form. D must also be chosen to have optimal overlap while at the same time keeping the computational load reasonable. L, called the spectral length, is 512 in most of the experiments reported in this thesis. The full sequence of a noise measurement is summarized in a flowchart in **figure 2.19**.

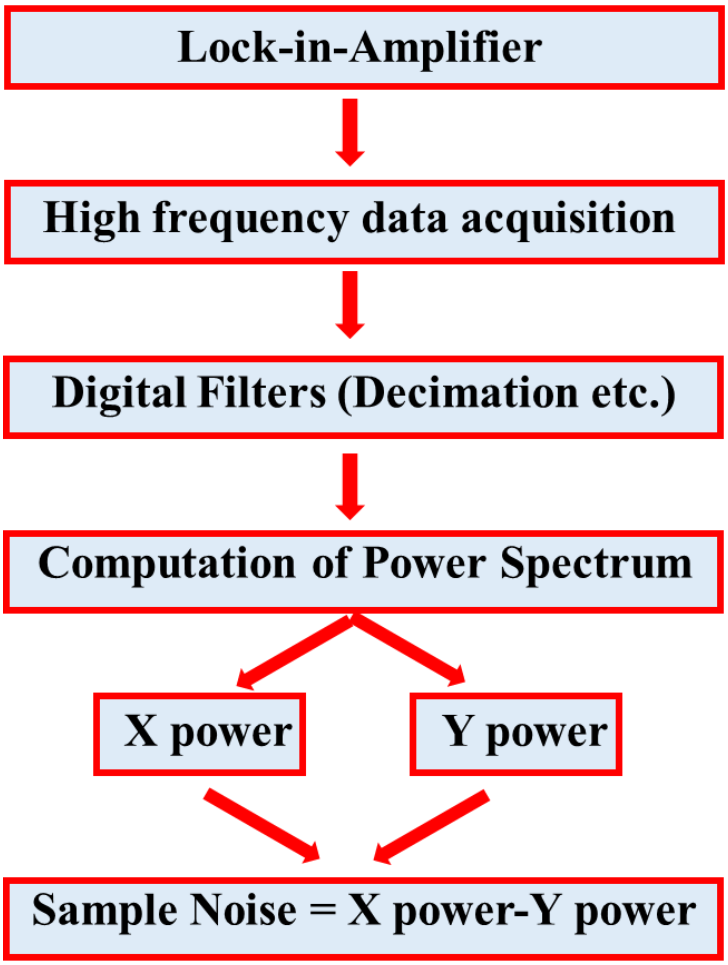


Figure 2.19. *Flowchart of the process involved in noise measurement.*

Chapter 3

Electronic transport and Noise spectroscopy in CVD Graphene FET on a lightly doped Si/SiO_2 substrate

3.1 Introduction

Electronic properties of Graphene[1,2] are studied mostly in the field effect geometry, where Graphene act as an electronic transport channel and to regulate the charge carriers efficiently a heavily doped (doping > 10^{20}/ cm^3) silicon/silicon dioxide substrate is used as a back gate. The Graphene/substrate interface can significantly affect the device's characteristics and performance because 2D systems are by definition fully surface-based and hence vulnerable to outside sources of disorder[59,63,106]. It has been found that a Graphene device's performance can be restricted by interface traps[107], Coulomb impurities[108], grain boundaries[63], or interfacial phonons[59]. The mobility of Graphene can be increased by orders of magnitude by totally removing the substrate or placing it on a trap-free substrate like hexagonal boron nitride (hBN) [3,49]. By encapsulating Graphene in hBN and utilizing graphite as a global gate electrode[109], one can detect strong interaction-driven phenomena like the Hofstadder butterfly[60] and fractional quantum hall effect[4] at the ultraclean limit. These, however, are still restricted to micron-scale devices and mostly employ a dry transfer[49] approach and scotch tape-based technique. It is still being investigated how to accomplish these in a large-area device. An option is chemical vapor-deposited large-area Graphene, however, the device's performance is severely constrained by the existence of inherent defects, grain boundaries, and chemical residues during the transfer process[84,110].

An essential tool for characterizing device performance and comprehending the impact of the time-varying disorder on the channel conductance in a field-effect device is low-frequency noise, often known as flicker noise. The interface states that are spatially close to the Graphene channel dominate resistance variations in Graphene[48,87,111,112]. The noise in Graphene devices are proposed to be explained by both number- and mobility fluctuation-based models. It is shown that fluctuations in the contacts can also play a major role in the noise performance in Graphene

devices. However, prior research on the noise in Graphene has mainly concentrated on the devices made on a degenerately doped Si/SiO_2 substrate[48,111,113–116], whereas it is crucial to fabricate Graphene devices on a lightly or moderately doped substrate[117–120], particularly for high-frequency applications, in order to integrate Graphene in the modern silicon industry. Graphene field-effect devices made on a lightly doped substrate have just a few transport investigations, but these devices have not yet been the subject of any research into low-frequency noise. Beyond the technical significance, it's critical to comprehend the device's operational region and look into the role of bulk defects in the resistance fluctuations seen in silicon-based field-effect transistors (FETs).

In this context, we report the electrical transport and low-frequency noise measurement on a large-area Graphene field effect transistor fabricated on a lightly doped (p+ doping ~ $10^{15}/cm^2$) Si/SiO_2 substrate. By varying the gate voltage, the substrate undergoes accumulation, depletion, and inversion, confirmed by capacitance (C) −voltage (V) spectroscopy. We observe a significant impact of the space-charge region formed at the Si/SiO_2 interface on the transport and noise behavior in the Graphene channel.

3.2 Experimental Details

3.2.1 Electronic transport in CVD Graphene on a lightly doped Si/SiO_2 substrate

CVD Graphene field-effect devices were fabricated using commercially available CVD Graphene (Graphenea, USA) on a lightly boron-doped (p+) Si/SiO_2 substrate (resistivity ~ 10 Ohm-cm) the doping concentration of the substrate is confirmed by the Capacitance voltage characteristics. The device was made by initially dry-etching the CVD Graphene with low-power oxygen plasma using an ICPRIE system with an oxygen flow rate of 20 SCCM and an RF power of 8 W for 15 s. Electrical contacts were defined using a laser writer using a positive photoresist, followed by deposition of Ti/Au (5/45 nm) in an e-beam evaporation system and lift-off process. The separation between the voltage leads was 70 μm, having a width of 50 μm as shown in **Figure 3.1a**.finally the device were bonded on a chip for the electrical transport measurement as shown in **Figure 3.1b**. The Raman spectroscopy of these device confirms single layer Graphene with negligible defects[12] **Figure 3.1c**.

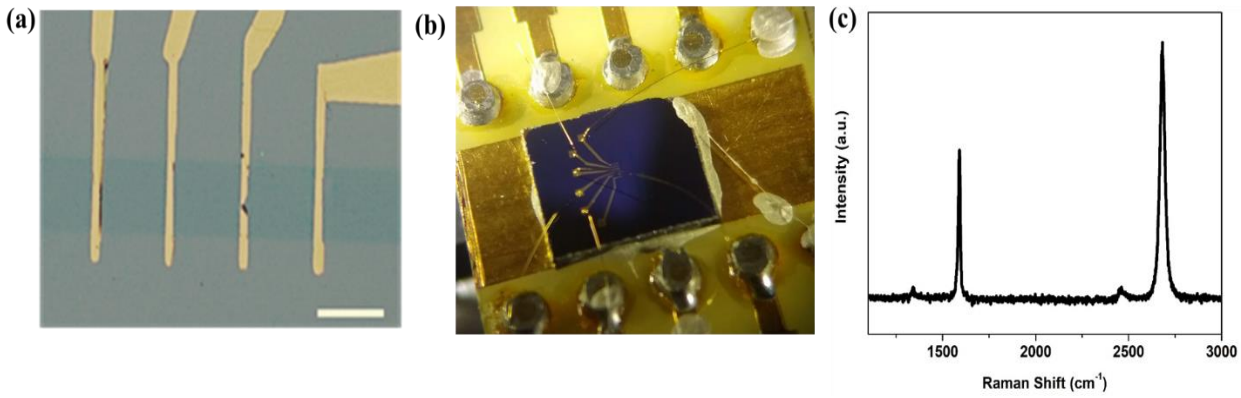


Figure 3.1. *(a) Optical micro-graph of the etched Graphene device. The scale bar is 50µm. (b) Optical image of the bonded device. (c) Raman spectra of the CVD Graphene exhibiting single Lorentzian peak around 2680 cm^{-1}, which confirms the single layer characteristics.*

For the CVD Graphene devices fabricated on a lightly doped Si/SiO_2 substrate at ambient temperature. I-V characteristics were linear across a range of gate voltages, indicating a good ohmic contact, as shown in **Figure 3.2a**. **Figure 3.2b** illustrates the typical variation of the four-terminal resistance (R) with the global back-gate voltage (V_{bg}). The R-V_{bg} characteristics show that the charge neutrality point (CNP) is 38 V, indicating that the device was unintentionally p-doped, probably as a result of the hole doping brought on by PMMA-based wet transfer[20,121,122]. Additionally, we have observed a hump in the R−V_{bg} characteristics, near $V_{bg} \sim 0$ V (**Figure 3.2b**). A similar hump was often noticed in low-mobility devices either due to contact-induced doping or

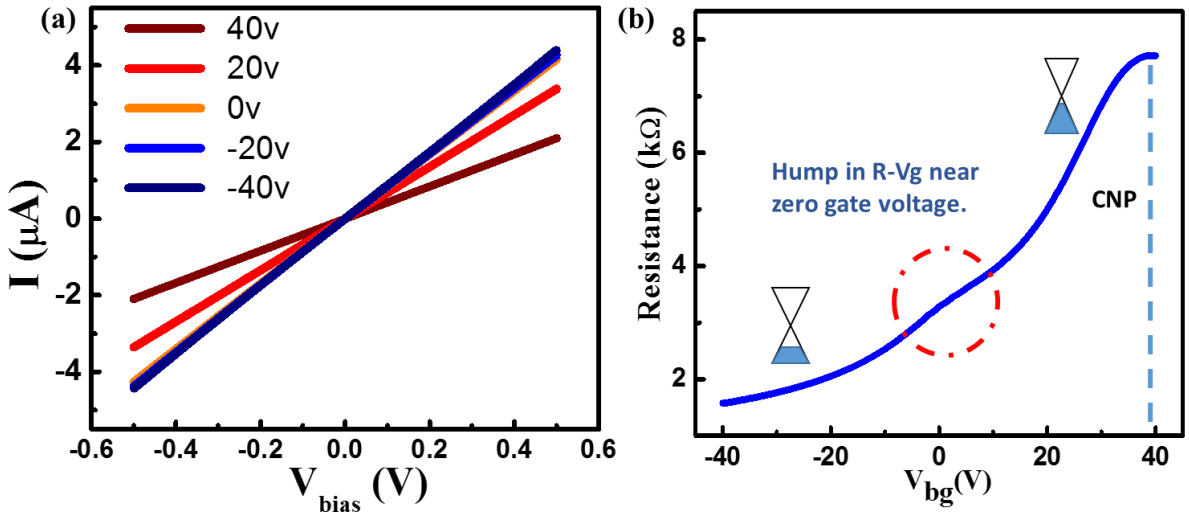


Figure 3.2. *(a) I-V characteristics of the device in different gate voltage shows a linear behavior conforming a good ohmic contact. (b) R−V_{bg} curve of the Graphene field-effect transistor (solid blue line), showing the charge neutrality point at ~38 V.*

due to the spatial inhomogeneity in the devices[123]. To understand the origin of the hump in the R-V_{bg} characteristics we have measured various Graphene devices on lightly doped substrate and in most of the devices we have found the origin of the hump around V_{bg} = 0 V (**Figure 3.3a**). Also two probe and four probe measurement of the device at different regions with varying length shows

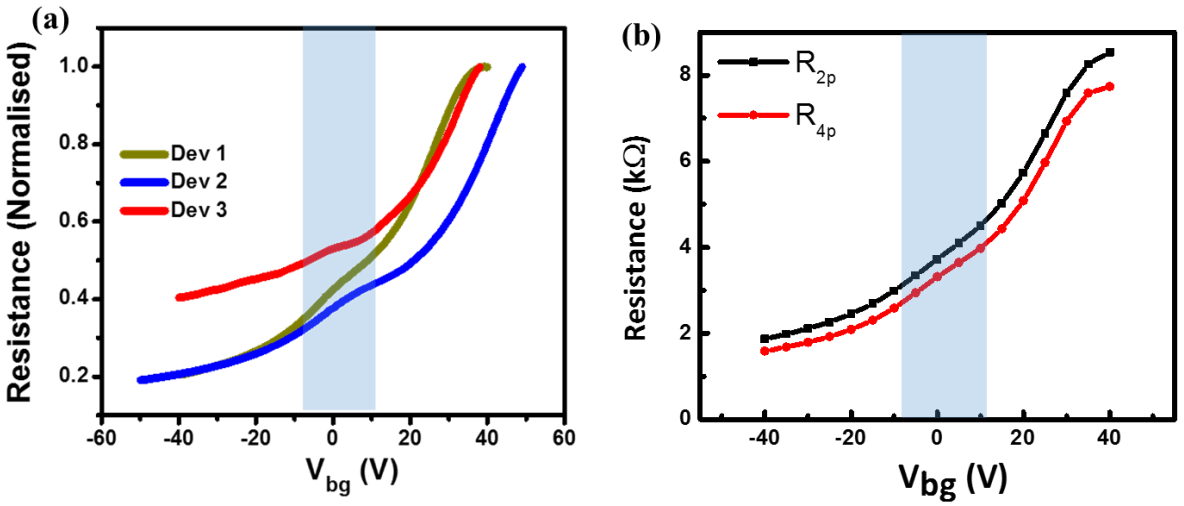


Figure 3.3. *(a) R-V_{bg} characteristics from three different devices at room temperature exhibiting the hump near V_{bg} = 0V.(b) The variation of resistance in two-probe (black) and four-probe (red) also shows the hump near zero gate voltage.*

the hump in the R-V_{bg} characteristics around zero gate voltage (**Figure 3.3b**), which rules out the possibility of contact induced doping and spatial inhomogeneity in the sample.

In some of the devices we have not observed any clear hump in the R-V_{bg} characteristics, but the derivative of the resistance with respect to the gate voltage shows a clear fluctuation around the 0 gate voltage, as shown in **Figure 3.4a**. This is possible due to large number of interfacial traps present in the system. To neutralize the traps, we have put ionic liquid ($LiClO_4$+PEO matrix), we observe two effects after adding the ionic liquid ($LiCO_4$) to the PEO matrix. In the beginning, the CNP is shifted from 42 V to 18 V, and the hump is recovered at zero gate voltage, as shown in **Figure 3.4b**. This is due to the neutralization of the interface traps by the ionic impurities and shifts the CNP towards lower gate voltage. All these observations points toward a different origin of the hump.

Temperature dependent R-V_{bg} characteristics of the device shows the hump near zero gate voltage. However, the effect of gate voltage on the resistance of Graphene weakens in the negative side

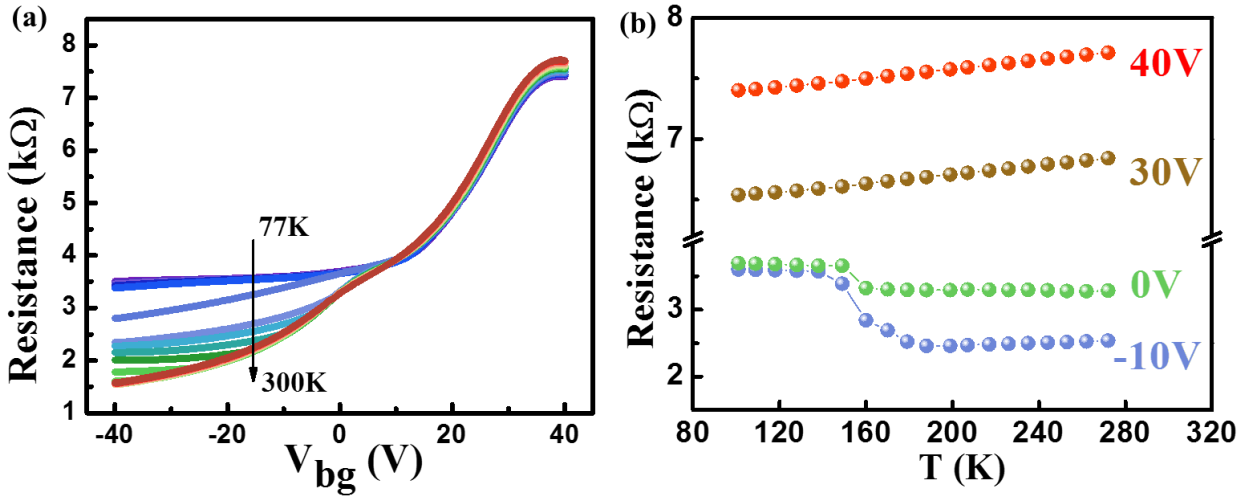


Figure 3.5: *(a) Temperature-dependent $R-V_{bg}$ curve of the Graphene FET device, showing flattening of the curve at low temperature in the –ve gate voltage. (b) The variation resistance with temperature for different gate voltages.*

and became almost non responsive below ~ 150 K, as can be seen in **Figure 3.5a** the temperature dependent resistance at different gate voltage on the positive side of the gate voltage shows, the resistance reduces with temperature, showing a metallic behavior (**Figure 3.5b**).

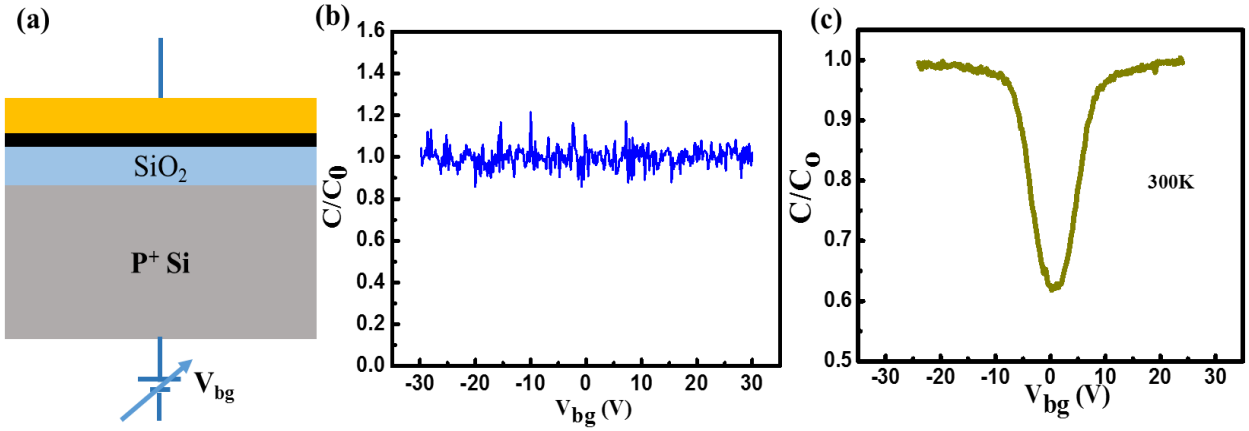


Figure 3.6. *(a) Schematic of the MOS structure (metal/Graphene/SiO_2/Si/metal) for the capacitance measurement. (b) Variation of capacitance with gate voltage for a highly doped silicon measured in MOS geometry. (c) Variation of capacitance with gate voltage for lightly doped Si/SiO_2 substrate at 300 K.*

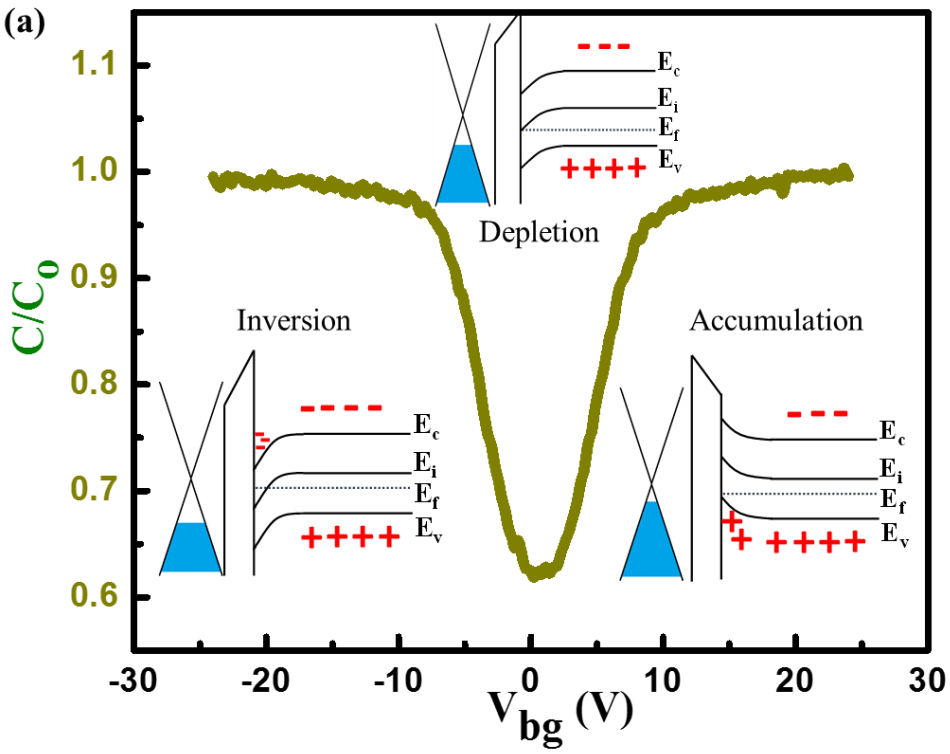


Figure 3.7. *(a) The schematic of the energy band diagram of the MOS capacitor on a lightly doped Si substrate against different gate bias condition is represented along with the change in the capacitance with varying gate voltage.*

3.2.2 Temperature dependent Capacitance – Voltage characteristics

To understand the effect of substrate on the transport properties of Graphene, we have look in to the capacitance vs gate voltage characteristics of our CVD Graphene on a lightly doped Si/SiO_2 substrate. We have performed the C-V measurement in a MOS capacitor configuration[124] (metal/Graphene/SiO_2/Si/metal) as shown in **Figure 3.6a**. The C-V measurement on a highly doped substrate shows no change in the capacitance upon varying the back gate voltage, shown in **Figure 3.6b**. The low frequency (100 Hz) C-V characteristics on a lightly doped substrate in MOS capacitor configuration shows a dip in the C-V characteristics at around ± 10 V, as shown in **Figure 3.6c.** The energy band diagram of our MOS capacitor is shown in **Figure 3.7a**. When the lightly doped silicon substrate is biased positively with respect to the Graphene, majority charge carriers from the lightly doped substrate starts to accumulate in the Si/SiO_2 interface without affecting the thickness of the dielectric. But when the gate bias gets lower and starts to approach towards zero gate voltage, the band bends downward and majority carriers starts to deplete and the effective capacitance decreases due to the depletion layer acting as a dielectric (**Figure 3.7a**). When the gate

voltage decreased further in the negative side the band bends even more downward so that the intrinsic level (E_i) at the surface crosses over the Fermi level (E_F). At this point the minority carriers start to accumulate at the Si/SiO_2 interface and thus inversion occurs, depletion charges are shielded resulting in an increase in the capacitance. At high frequencies (>100 kHz), the minority electrons cannot follow the change in gate voltage and the inversion layer does not form.

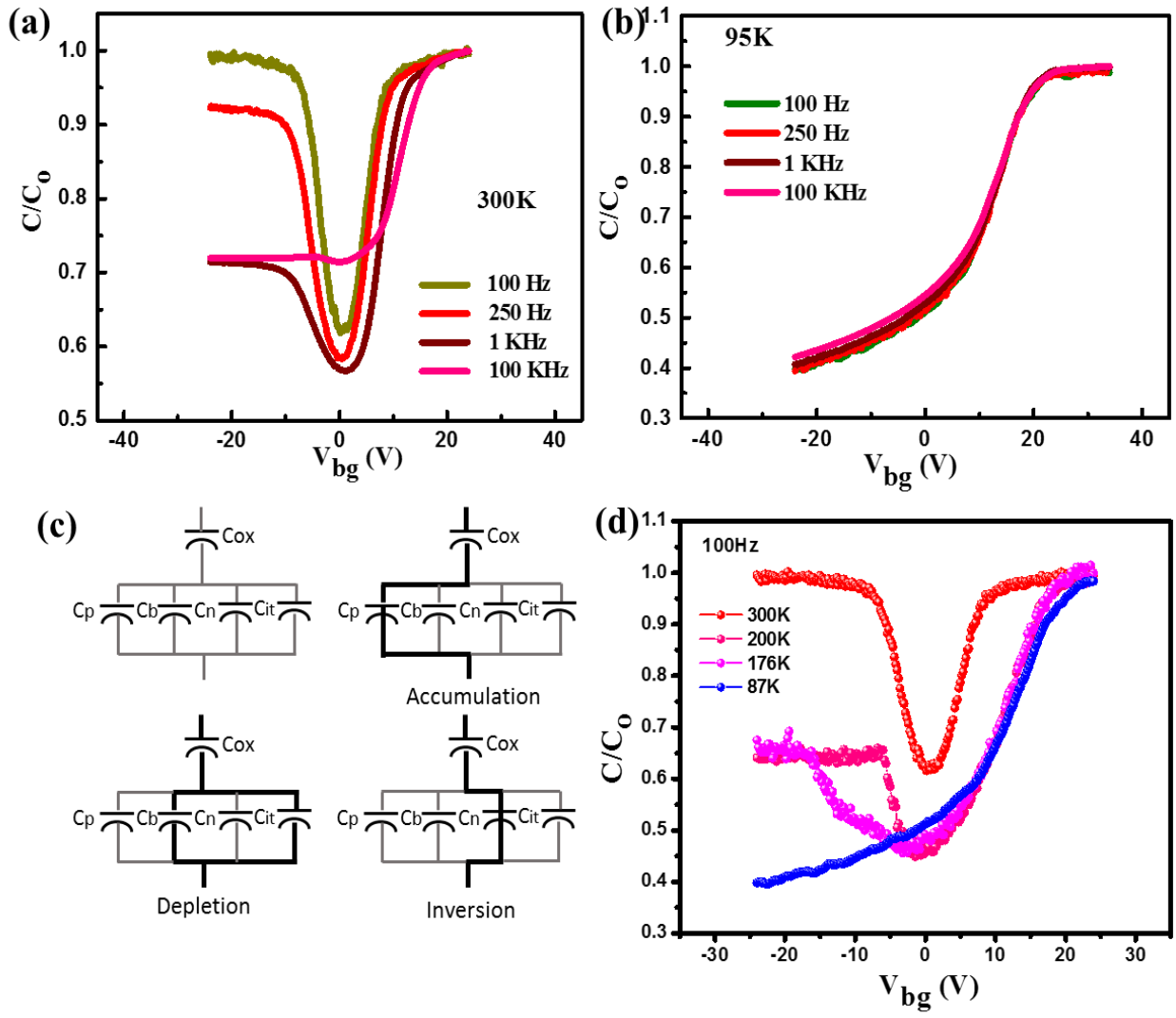


Figure 3.8. *(a), (b) Variation of capacitance with gate voltage for lightly doped Si/SiO_2 substrate with different frequencies at 300 K and 95 K. (c) Equivalent capacitance circuit for the MOS device for different substrate conditions as a function of the gate bias. (d) Temperature dependent C-V characteristics of Si/SiO_2/Graphene/Au MOS capacitor at 100 Hz.*

The capacity to add carriers to the Graphene channel is reduced when the depletion region forms due to an increase in the effective thickness of the gate dielectric and a drop in gate capacitance. Which results in the formation of hump in the R-V_{bg} characteristics. Haddad et al[117]. noticed a similar pattern of behavior and utilized the drift-diffusion model[125] to explain it using a thinner (20 nm) SiO_2 dielectric layer. The transport behavior is greatly influenced by both the Graphene quantum capacitance and the depletion capacitance. Due to the SiO_2 layer's thickness (300 nm), the quantum capacitance[126] in our situation plays a minor role in comparison to the oxide and depletion capacitances. The variation in the C-V characteristics with frequency at 300 K and 95 K (**Figure 3.8a, b**) further reveals the interfacial traps' considerable influence[127–129]. The equivalent circuit for the MOS capacitor in **Figure 3.8c** can help make this more evident. The combination of the oxide capacitance, C_{ox}, in series with the four parallel capacitances, C_p, C_b, C_n, and C_{it}, which are caused, respectively, by the hole charge density, electron charge density, bulk space-charge density, and interfacial trap charge density[130], can be used to represent the total capacitance. As in the accumulation (inversion) region, Q_p (Q_n) is the dominant charge carrier, C_p (C_n) becomes significantly large, approaching short circuit, and hence, the equivalent capacitance effectively equals to the oxide capacitance, C_{ox}. In the depletion region, however, the bulk and interface capacitances dominate, as both Q_n and Q_p become significantly small, giving rise to the overall capacitance as C_{ox} in series with the parallel combination of C_b and C_{it} (**Figure 3.8c**). **Figure 3.8d** depicts capacitance variation with gate voltage at 100 Hz for various temperatures. The red curve corresponds to the C-V curve at 300 K, where three distinct zones may be seen. The oxide capacitance is equal to the capacitance in the accumulation and inversion areas. Lowering the temperature reveals that the inversion capacitance cannot reach the oxide capacitance due to a lack of thermally produced minority carriers. When the temperature falls below the freeze-out[118] temperature (150 K), the depletion area expands and enters the deep-depletion region[127,130], where the gate loses its capacity to induce charge carriers in Graphene, as a result the flattening in the R-V_{bg} characteristics is observed at –ve gate voltage at low temperature.

3.2.3 1/f Noise in Graphene FET on a lightly doped Si/SiO_2 substrate

Low frequency 1/f noise in the Graphene field effect transistors fabricated on a lightly doped substrate was measured using lock in amplifier based ac four probe technique as described in detail in **section 2.3** of this thesis. The excitation current was kept very low about 1 μA to avoid unnecessary heating of the sample. Other nonlinearity of the sample were verified by the quadratic dependence of voltage/current noise at a fixed resistance R. The background noise was also

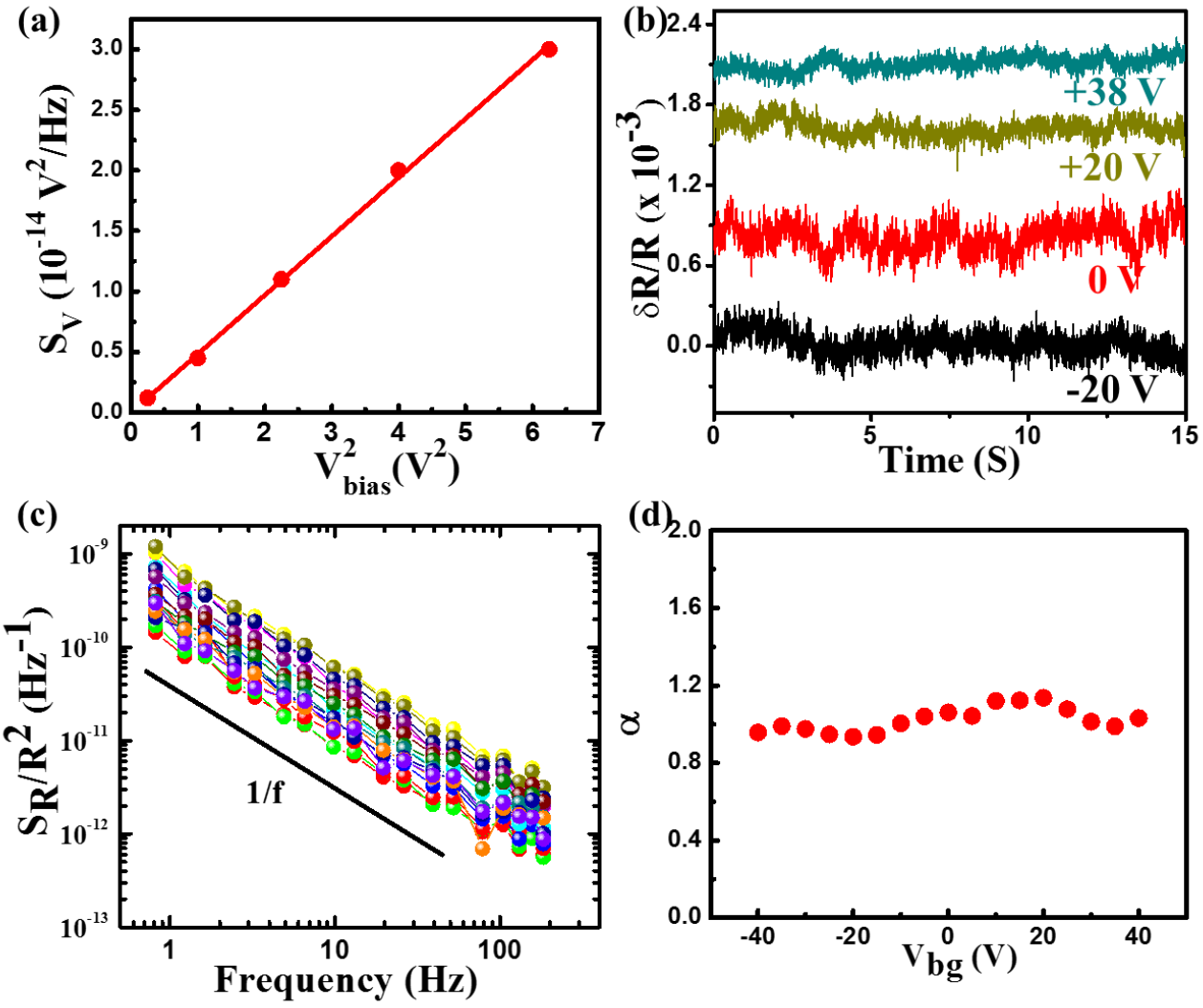


Figure 3.9. *(a) Variation of noise power spectral density, Sv with V_{bias}^2, exhibiting linear behavior expected for Ohmic contact. (b) Time-domain resistance fluctuation at different V_{bg}. (c) Typical noise power spectra S_R/R^2 at various V_{bg}, showing 1/f characteristics. (d) Variation of α with V_{bg}, calculated from the linear fit of the 1/f noise data.*

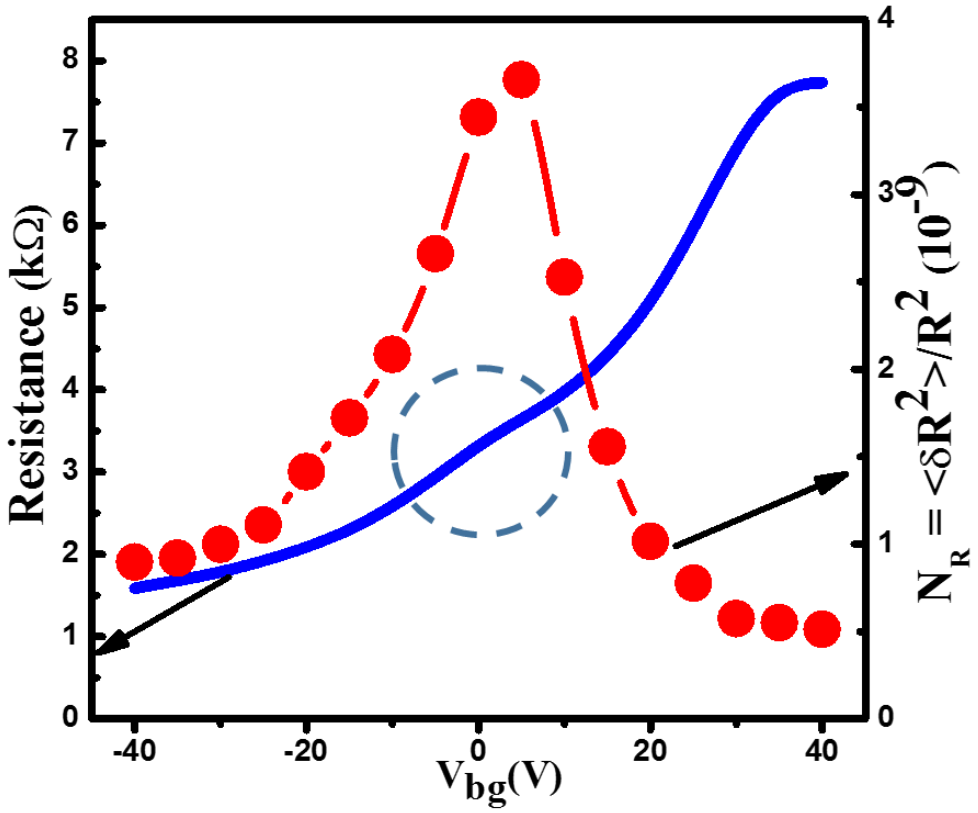


Figure 3.10. *Variation of normalized noise PSD, integrated over the measured frequency bandwidth (N_R) (red data points) and Resistance (blue solid line) with V_{bg}. A clear increase in noise is observed around 0V.*

measured simultaneously and subtracted from the total noise. Before measuring the actual sample thermal noise of a standard resistance is measured in the same contact configuration to calibrate the setup.

A carrier frequency of 1.66 kHz was used for the noise measurement, and the time-dependent output of the lock-in amplifier was digitalized. Next, the signal underwent multistage decimation to remove the effects of higher harmonics of the power line and other undesirable frequencies, and then the power spectral density (PSD) [131] was calculated. During the noise measurement the device was kept at a constant gate voltage and the time varying resistance fluctuation is recorded using high frequency data acquisition card present in the MFLI lock-in. The time series data of our device at different gate voltage is shown in **Figure 3.9c**. The normalized noise PSD at different gate voltage (shown in **Figure 3.9b**) follows $\frac{1}{f^{\alpha}}$ **,** where α varies form 0.8-1.2 **(Figure 3.9d**).

Typically, the normalized power spectral density (PSD) of resistance noise follows the empirical Hooge's relation, $S_R(f) = \frac{\gamma_H R^2}{nA_G f^\alpha}$, where A_G is the area of the sample between the voltage probes, n is the carrier density, and γ_H is the empirical Hooge's parameter. Here, instead of focusing on the amplitude of noise power at a particular frequency or γ_H we analyzed the total variance of resistance fluctuation,

$$N_R = <\delta R^2>/R^2 = \frac{1}{R^2}\int S_R(f)df \ldots\ldots\ldots\ldots\ldots\ldots (3.1)$$

Which is essentially the normalized noise PSD integrated over the experimental bandwidth[132]. The normalized noise PSD (N_R) of the device as a function of gate voltage is shown in **Figure 3.10**. We have observed a peak in the normalized noise PSD around the zero gate voltage, where the hump in the resistance is observed in the R-V_{bg} curve and the decrease in the capacitance is observed during the C-V measurement. The time series data of δR/R (**Figure 3.9b**) corroborate the peak in the normalized noise at V_{bg} = 0 V.

3.3 Results and Discussion

Resistance fluctuations in Graphene were shown to arise either from the contact or from the trapping−detrapping processes primarily from the interfacial traps. Previous experiments on the noise spectroscopy in Graphene field effect transistors proposed two mechanism[132]. First, the charge exchange noise (Nch-ex), which originates mostly due to the trapping−detrapping processes between Graphene and the underlying traps present in the SiO_2 or with the adsorbents present over the sample, of which a quantitative expression was developed based on the correlated number and mobility fluctuation models[111,132–134]. Another type of noise, known as configuration noise (Nconfig), where no charge exchange will occur; however, fluctuations in the occupancy of the traps may change the scattering cross-section over time and cause fluctuations in resistance based on the local interference model developed by Pelz and Clarke[90]. Due to the fact that these two contributions happen separately, the overall normalized noise magnitude may be expressed as,

$$N_R = N_{ch-ex} + N_{config} = A(n_{it}, T)\left(\frac{d\sigma}{dn}\right)^2 + B(n_{ir}, T)N_c(n) \ldots\ldots (3.2)$$

where σ is the conductivity, n is the carrier density of Graphene, n_{it} is the density of interfacial traps closed to Graphene where charge exchange occurs between Graphene and the traps and n_{ir} is the density of traps responsible for mobility fluctuations without any charge exchange processes. It is evident that N_{ch-ex} is proportional to the square of the differential mobility ($\sim(d\sigma/dn)^2$) and the density independent proportionality constant, A, will be proportional n_{it} and follows the temperature (T) dependence according to the McWhorter's activated model[88] . The density dependent part of the second term,$N_c(n) = (|n|/n_\Delta)^\gamma$) and 1 for $|n| > |n_\Delta|$ and$|n| < |n_\Delta|$, respectively, where the parameter n_Δ denotes the characteristic density below which the charge distribution in Graphene is inhomogeneous due to the presence of charge puddles. The parameter γ varies between -1 and -2 for single layer Graphene and signifies the enhanced screening ability with increasing density.

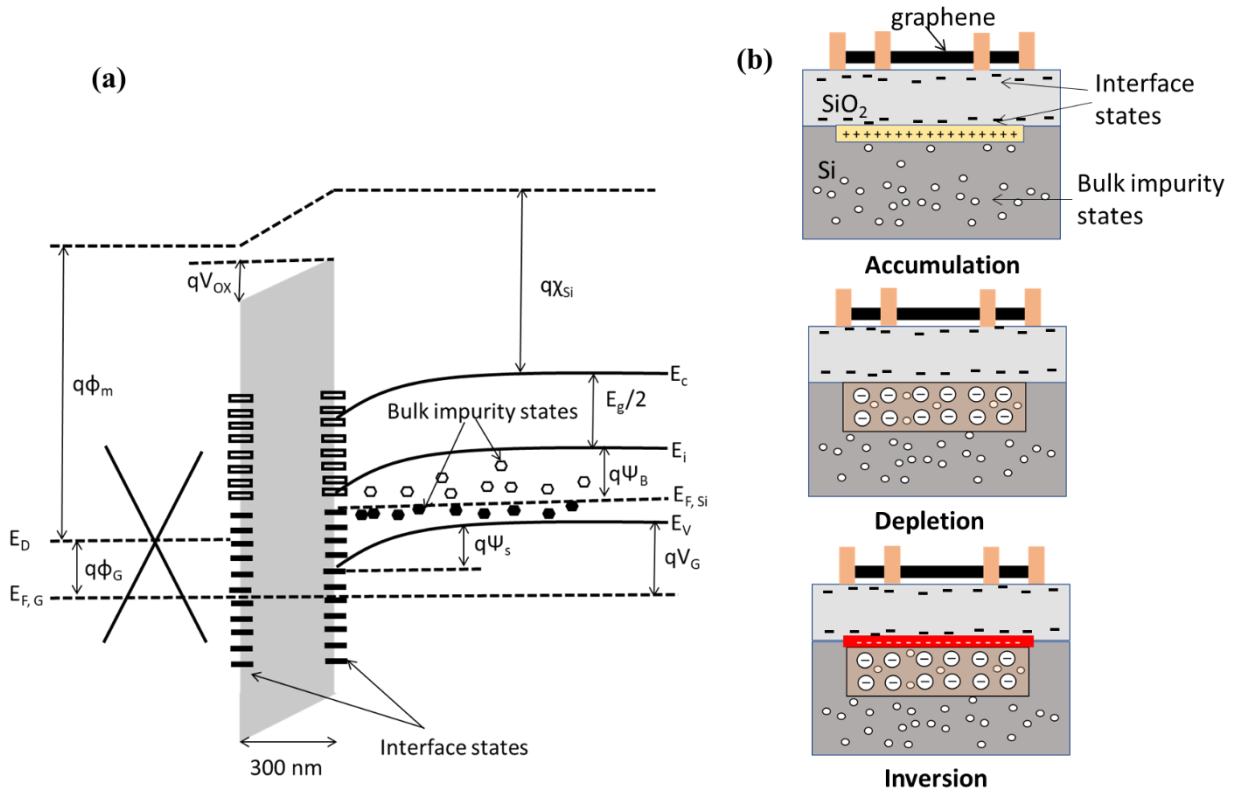


Figure 3.11. *(a) Schematic energy band diagram of Graphene/SiO_2/Si (p+) structure with different band parameters, showing the interface and bulk impurity states inside silicon. (b) Schematic diagrams of three different regime obtained by the application of gate voltage. The effect of bulk defects become important only in the depletion region as there no charge layer formed at the SiO_2 /Si interface to screen any charge fluctuations inside the bulk of the silicon.*

The observed dip in noise at the CNP, coupled with the modest rise with n, characterizes the distinctive behavior of low-mobility Graphene devices. In these devices, the dominant source of charge exchange noise arises from interfacial traps, overpowering the second term in our CVD Graphene devices[132]. While the noise peak near zero gate voltage cannot be solely explained by models based on interfacial traps, our findings suggest a potential association with the formation of the depletion region. Consequently, bulk defects may be accountable for the fluctuations in resistance.

The energy band diagram of the Graphene/SiO_2/Si/Metal structure is depicted in the **Figure 3.11**. Whenever a gate voltage (V_{bg}) is applied, the energy bands are either pushed upwards or downwards depending on the sign of the gate voltage. As shown in the figure, when a negative gate voltage is applied to the bulk silicon the energy bands will be pushed upward which results into downward bending of the energy bands ($q\psi_s$) at the silicon-silicon dioxide interface. Through the capacitive coupling the Fermi level in the Graphene channel shifts ($q\phi_G$) due to the application of gate voltage. This results in to a potential difference across the SiO_2 which results into upward tilting (qV_{ox}) of the energy bands toward the gate[117,127] From the energy band diagram one can write down the energy conservation equation as

$$-q(V_G - V_{Ch}) + q\psi_B - q\psi_S + \frac{E_g}{2} + q\chi_{Si} - qV_{OX} - q\phi_m + q\phi_G = 0$$

Where, χ_{Si} is the silicon affinity, E_g is the band gap of silicon, ϕ_m work function of Graphene, V_{OX} is the voltage drop across SiO_2, ϕ_G is the Graphene channel potential, ψ_S is the surface potential, and V_G is the applied gate voltage. By solving the equation numerically and using the drift diffusion model, it is possible to obtain the transport characteristics in three different regions[4]. Interfacial traps are found at both Graphene/ SiO_2 and SiO_2/Si interfaces, as well as within the oxide dielectrics[127]. Additionally, SRH-type defects[135] contribute to generation-recombination (GR) noise[136–139] within the bulk of the silicon.

In regions of accumulation or inversion, the impact of bulk defects is negligible compared to interfacial traps. This is because the accumulation or inversion layer effectively screens any charge fluctuations of this nature. However, in the depletion region, three significant effects come into play. Firstly, the effective carrier density of Graphene undergoes a nearly twofold change, potentially amplifying the configuration noise term in Equation 3.2 due to reduced screening.

Secondly, the Graphene channel experiences notable coulomb fluctuations due to GR noise within the substrate bulk, thereby increasing configuration noise through mobility fluctuations in

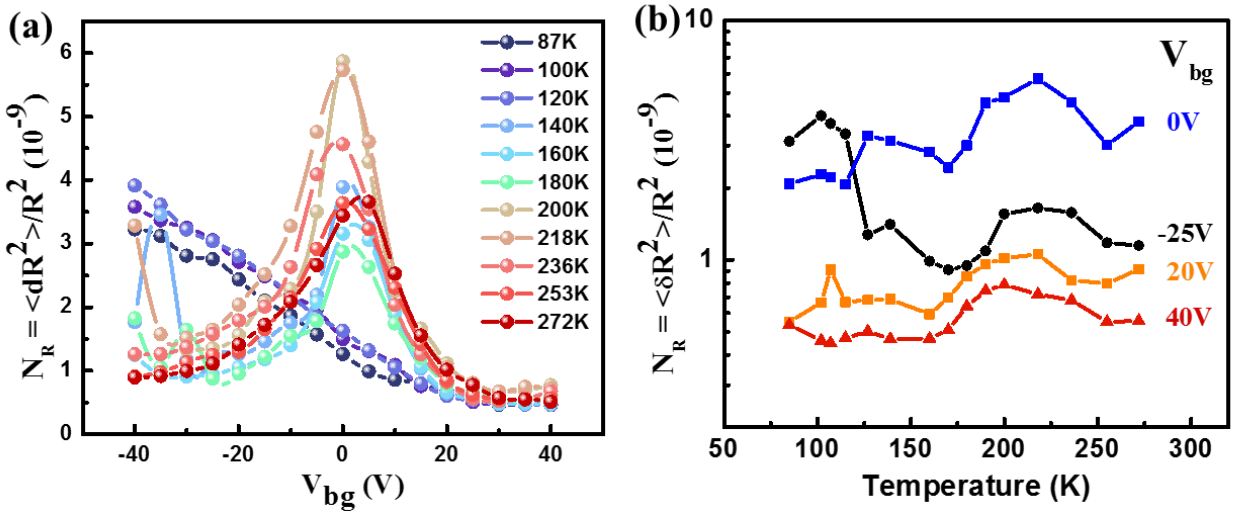


Figure 3.12. ***(a)*** *Variation of normalized noise PSD (N_R) with V_{bg} for different temperature.* ***(b)*** *Temperature dependence of N_R for different fixed V_{bg}.*

Graphene[140,141]. Lastly, the electric field induced by the depletion region may modify the potential of interfacial traps, further enhancing the noise[142–144].

Currently, the challenge lies in untangling the contributions from different mechanisms and obtaining a quantitative estimate of remote defects through an analytical model. The temperature-dependent noise data reveals two noteworthy features. Firstly, the noise peak near zero gate voltage diminishes below T ~ 150 K (see **Figure 3.12a**). Secondly, noise at various gate voltages exhibits non-monotonic behavior with temperature[145]. The disappearance of the noise peak at lower temperatures is associated with the carrier freeze-out phenomenon in the silicon substrate. At these lower temperatures, the unavailability of thermally generated minority carriers from the bulk silicon prevents the formation of an inversion layer, plunging the SiO_2/Si interface into a deep depletion region. Consequently, in this freeze-out region, the generation-recombination (GR) noise decreases due to insufficient carriers for the trapping-detrapping process, leading to the disappearance of the peak.

The rise in noise amplitude with gate voltage in the freeze-out region, where gating ability diminishes, can be explained as follows. In the absence of an inversion layer in the deep depletion region, the gate electric field is not effectively screened. This results in a reduction of the trap potential near the Graphene/ SiO_2interface, causing noise to monotonically increase with the gate

electric field due to heightened noise from interfacial traps. The temperature-dependent normalized noise power spectral density (PSD) for different gate voltages is illustrated in **Figure 3.12b**, clearly indicating a non-monotonic increase with temperature, reaching a maximum in the temperature range of 200 K to 230 K.

In the inversion region (V_{bg} = -25V, **Figure 3.12b**), a sudden rise in noise with decreasing temperature below T = 150 K is observed, in addition to the maximum at ~220 K. Previous studies on the temperature dependence of noise in Graphene on a heavily doped substrate show activated behavior with temperature[132], suggesting a significant role of trapping-detrapping processes at the interface following the Dutta & Horn model[77]. The non-monotonic noise behavior in our case further implies that the influence of the bulk substrate is more pertinent compared to interfacial traps. Since charge fluctuations within the substrate are linked to the mobility of charge carriers, which exhibits nonmonotonic behavior with temperature, this could be a plausible explanation for

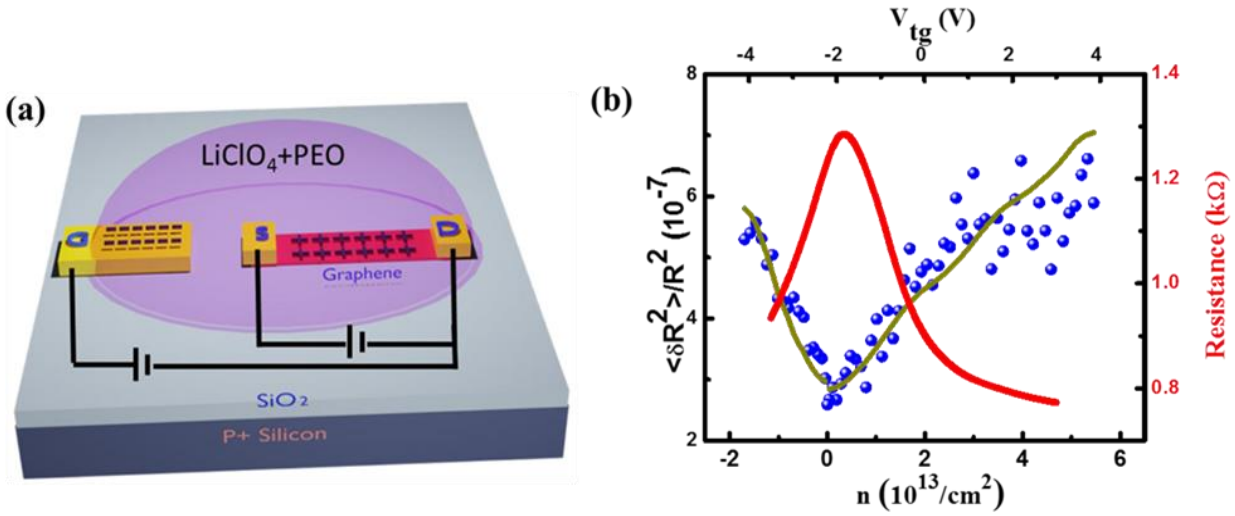


Figure 3.13. *(a) Schematic of the ionic liquid gated CVD device. (b) Variation of Resistance (red line) and noise (blue dots) as a function of carrier density of liquid ion gated Graphene field effect transistor. The green solid line indicates the fitting with the model proposed.*

the observed noise behavior in our Graphene device.

To strengthen our assertion, we conducted noise measurements on a top-gated Graphene device, fabricated on the same wafer employing an ionic liquid, $LiClO_4$+ PEO matrix, as the top gate dielectric, as illustrated in **Figure 3.13a**. In the presence of an ionic liquid, the application of potential leads to the formation of a Debye layer, approximately 1-2 nm thick, at the Graphene/liquid interface. This layer facilitates the induction of a large number of charge carriers

with a small gate voltage[146]. The Resistance (R) vs. top gate voltage (V_{tg}) characteristics of the top-gated device, revealing the charge neutrality point (CNP) at approximately -1.9V, are presented in **Figure 3.13b**. Subsequent noise measurements on the device are depicted in **Figure 3.13b** (blue circles), revealing the absence of a peak near zero gate voltage, unlike the observation in the back-gated device.

The normalized noise (N_R) as a function of gate voltage shows a minimum at the CNP and increases on both sides of the CNP, reaching saturation at high density on the positive side. Consistent with prior findings[132,147], a similar dip in noise amplitude was observed in both top-gated and back-gated Graphene field-effect devices. The density-dependent noise data can be effectively fitted with the equation $N_R = A(T)(\partial\sigma/\partial n)^2 + C(T)$, where the dominant first term represents the contribution from charge exchange noise due to interfacial traps. The second term, independent of density, may originate from contact noise or configuration noise, as elucidated in previous reports[147,148].

3.4 Summary

- Experimental study on the electronic transport and low-frequency noise characteristics of a large-area CVD Graphene field-effect transistor fabricated on a lightly doped silicon substrate (doping concentration ~ $10^{15}/cm^3$). Key findings include the observation of a hump in the resistance vs. gate voltage characteristics at room temperature, attributed to reduced gate capacitance due to the formation of a depletion region at the SiO_2/Si interface, particularly impacting low-frequency noise near V_{bg} = 0V.

- Temperature-dependent noise measurements, along with capacitance and resistance measurement down to 77 K, establish a direct correlation between the observed noise and the formation of the depletion region. The proposed mechanisms for the noise involve bulk charge fluctuations within the depletion region and modulation of the energy level of interface traps, contributing to mobility fluctuations in the Graphene channel.

- Measurements on a top-gated device exhibiting behavior explainable by charge exchange processes between Graphene and interfacial traps near the surface. The overall conclusion

emphasizes the sensitivity of Graphene field-effect transistors to remote bulk charge fluctuations in lightly doped substrates. This findings is crucial not only for integrating Graphene with existing silicon technology but also for providing fundamental insights into the impact of remote interfaces on electron transport in Graphene.

Chapter 4

Functionalization of Graphene

4.1 Introduction

Graphene's exceptional properties, including rapid charge transport and thermal conductivity, make it a promising material for electronics. However, the lack of a band-gap in pristine Graphene hinders its application in digital electronics. To address this, researchers explore precise electronic manipulation through doping. Strategies include substitutional doping, introducing stability but disrupting the honeycomb structure, and reversible doping with physically adsorbed gaseous molecules.

The introduction of molecular derivatives with electron donating or withdrawing groups offers versatile avenues for tailoring electronic properties, introducing p or n doping and inducing a small band gap. Integrating Graphene with photosensitive semiconducting nanoparticles yields highly sensitive phototransistors. Additionally, decorating Graphene with magnetic molecules produces materials with tunable magnetic behavior, enhanced electronic transport, and spin-polarized currents, holding promise for spintronic applications. This dynamic field showcases the evolving landscape of Graphene-based materials, pushing the boundaries of electronic applications and material science.

In this section of the thesis, our focus is towards the exploration of hybrid molecular devices. Molecules have garnered significant attention owing to their low dimensionality, unique functionalities, synthetic tailorability, and the ability to self-assemble and recognize. One intriguing category of molecular systems investigated in this context is the spin crossover molecules (SCO). These molecules exhibit the ability to transition between high spin and low spin states in response to external stimuli such as temperature, light, and pressure.

However, a notable challenge arises from the weak coupling between these organic molecules and metallic electrodes, resulting in low conductivity. This limitation becomes a significant bottleneck when considering their application in electronic devices. In our research, we addressed this challenge by integrating these low-conductivity molecules with highly conductive Graphene and

reduced Graphene oxide, creating a functional device. Through the manipulation of gate voltage, temperature, and magnetic field, we successfully tuned the cooperativity among the molecular systems. The ability to dynamically adjust the cooperative behavior of the molecular system offers a pathway for tailoring the device's performance and the desirable tunable hysteresis effect, highlighting the potential of this hybrid molecular device as a versatile and adaptable component in the landscape of emerging electronic technologies

4.2 Experimental Details

4.2.1 Synthesis of SCO nanoparticles

The synthesis of the $[Fe(Htrz)_2(trz)]BF_4$ nanoparticle network utilized an adapted reverse micelle technique previously employed by Coronado et al.[149] and Roubeau et al. [150] The procedure involved the preparation of two separate microemulsions at room temperature:

(i) In the first microemulsion, an aqueous solution of $Fe(BF_4)_2.6H_2O$ (0.3 mL, 1 M) was created by dissolving 101.3 mg of $Fe(BF_4)_2.6H_2O$ in 0.3 mL of deionized water. To prevent Fe(II) oxidation, a pinch of ascorbic acid was added. This solution was then introduced into a 10 mL n-octane solution of sodium dioctyl sulfosuccinate (NaAOT) (1.35 g) and stirred for 30 minutes, resulting in a stable microemulsion. A co-surfactant, 0.402 g of behenic acid, was added and stirred for an additional hour.

(ii) The second microemulsion involved the preparation of an aqueous solution of 1,2,4-triazole (Htrz) ligand (0.3 mL, 3 M) by dissolving 62.16 mg of Htrz in 0.3 mL of deionized water. This solution was then added to another NaAOT (1.35 g) and octane solution (10 mL) with continuous stirring for 30 minutes to achieve a stable microemulsion. After filtering both microemulsions, the second microemulsion was introduced into the first, and a continuous stirring process ensued. Over time, the micellar exchange led to the formation of $[Fe(Htrz)_2(trz)]BF_4$ nanoparticles (NPs), transforming the solution into a clear, deep pink suspension. To halt the reaction, 50 mL of acetone was added after 30 minutes, followed by centrifugation. Subsequently, the excess surfactant was removed through three washes with ethanol. The resulting washed nanoparticles exhibited a purple hue and were ultimately dispersed in ethanol.

The SCO nanoparticles were synthesized by Chinmoy Das from Dr. Pradip Chakraborty's group, IIT Kharagpur. The as synthesized nano-particles shows a reversible color change during the

heating/colling process (**Figure 4.1b**). The change in the color during the process signifies the well reported spin transition in this nano particles. The DLS measurement on these nanoparticles shows that the average particle size is of the order of 30-40nm.

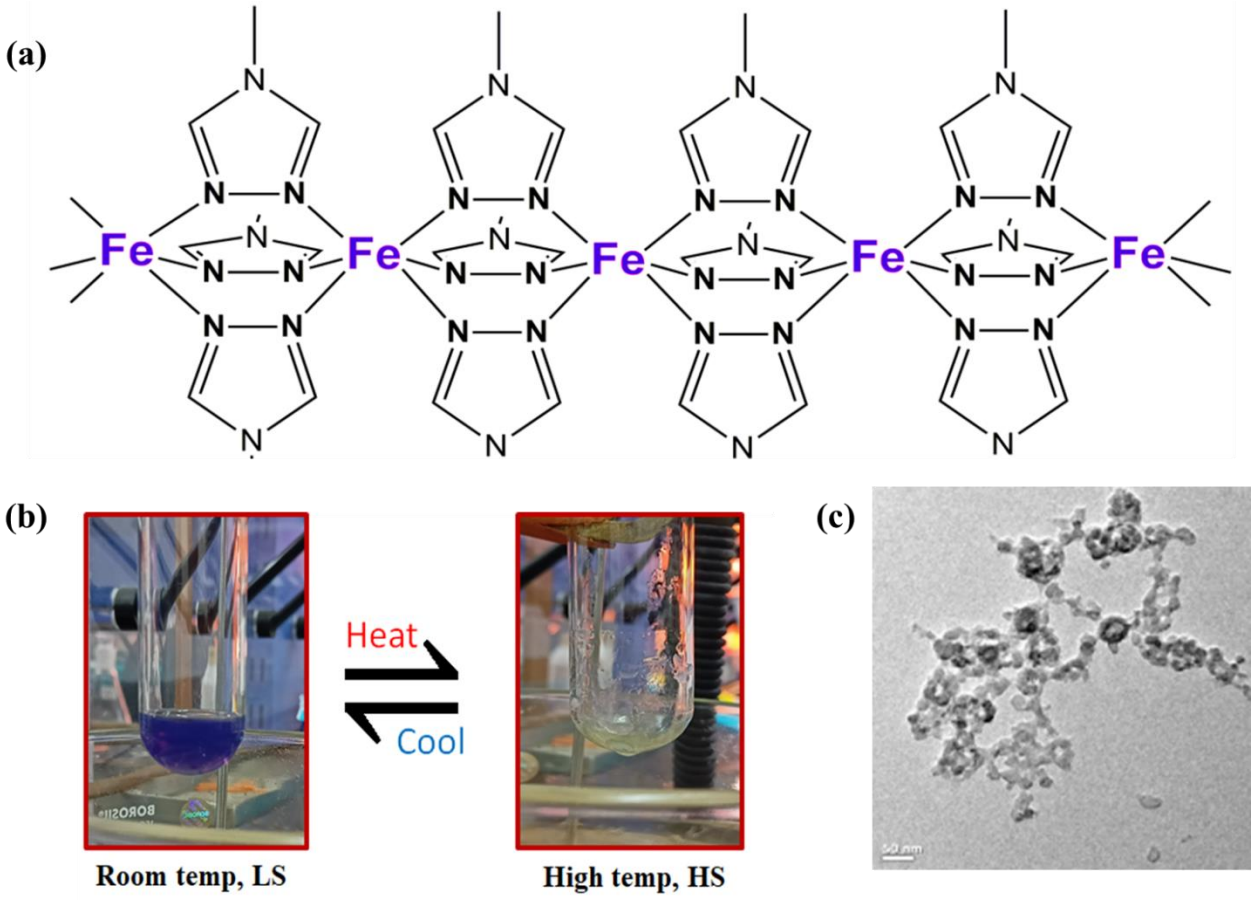


Figure 4.1. *(a) Structure of the Molecule ([Fe(Htrz)2(trz)]BF4) (b) SCO nanoparticle showing reversible color change due to heating/cooling shows thermal spin state transition (c) TEM image of the SCO nan particle.*

4.2.2 Preparation SCO/Graphene hetero-structure

Here, we investigated the charge transport in two hybrid system: (i) Graphene/ SCO hybrid system in the Field effect geometry, and (ii) rGO-SCO composites. For Graphene/SCO hybrid system in field effect geometry we have simply drop-casted and spin coated the nanoparticles over the Graphene field effect transistor. In the second case where we have prepared a composite system using rGO and SCO the preparation procedure is as follows. A 10 mg sample of Graphene oxide (GO) powder, obtained from GrapheneaTM, was dispersed in 50 ml of ethanol using ultrasonication for two hours to achieve layer exfoliation. Simultaneously, a few drops of the as-synthesized $\underline{Fe(Htrz)_2(trz)}$ nanoparticles (NPs) were diluted in 10 ml of ethanol in a separate

container. Subsequently, the GO suspension underwent heating to 60°C with continuous stirring to facilitate attachment. The $Fe(Htrz)_2(trz)$ nanoparticle solution was gradually introduced to this mixture. Following this, a washing step, centrifugation at 10,000 rpm, and filtration were performed to eliminate excess solvents. Given that GO possesses numerous functional groups on its basal plane and a negatively charged surface environment, the spin crossover (SCO) nanoparticles could readily attach to the GO surface through electrostatic interactions. Additionally, they had the capability to intercalate within the interlayer separations of GO. The resulting composite was subjected to further thermal reduction in the presence of ultra-high-purity (99.9%) H2 gas. This process occurred within a closed quartz 3-zone chemical vapor deposition (CVD) furnace at a temperature of 200°C for four hours, completing the reduction process and forming the SCO-reduced Graphene oxide (rGO) heterostructure.

4.3 Characterizations rGO/SCO hybrid system

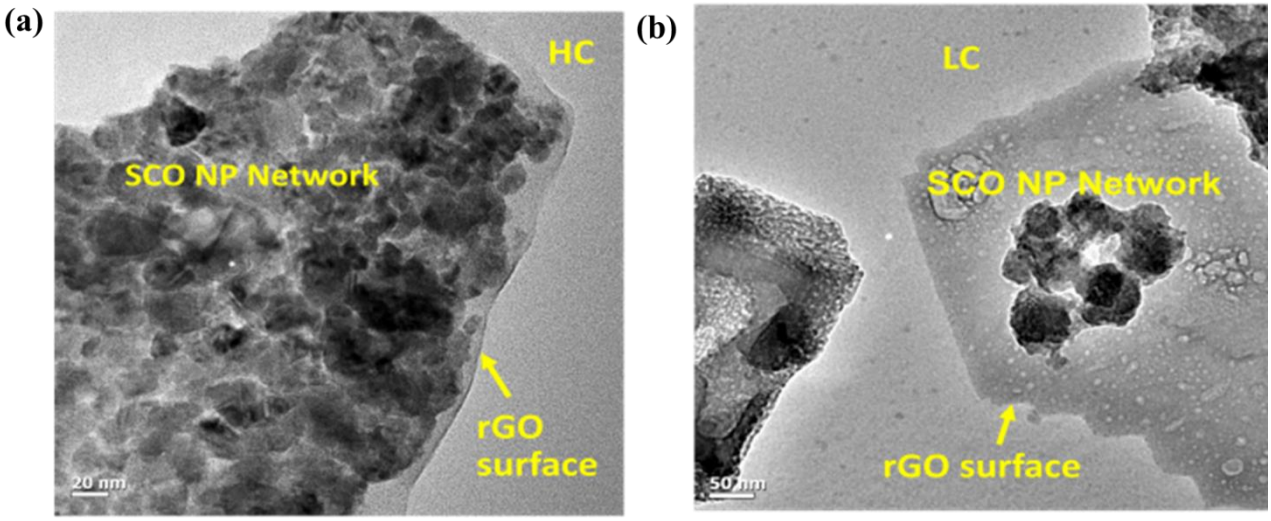


Figure 4.2. *TEM image of the nano particle attached with the rGO surface (a) High concentration of SCO (b) Low Concentration of SCO*

4.3.1 Structural Morphology from TEM image

In **Figure 4.1c**, the TEM micrograph reveals the pristine SCO nanoparticle network interconnected. **Figure 4.2** depicts the hybrid structure's overall morphology after attaching the SCO nanoparticle network to the rGO surface, with a thin rGO plane visible in the background. The transparency of the rGO layer indicates a few layers.

In the high-resolution image of the HC sample (**Figure 4.2a**), SCO nanoparticles densely cover the rGO surface, extending over almost the entire area. **Figure 4.2b** demonstrates a change in coverage area tunability, showing a low concentration sample. In the LC, controlled dense overlapping results in a uniform network. In both cases, no dense nanoparticle network is observed outside the rGO layer, confirming the synthesis's controlling ability.

4.3.2 Charge transfer and bonding state analysis

We conducted XPS analysis on the SCO-rGO nanocomposite to discern elemental oxidation states and the functionalization process, comparing it with pristine rGO through deconvolution of high-resolution peaks. In the C 1s spectra of the SCO-rGO composite (**Figure 4.3a**), after deconvolution, we observed the emergence of an additional C-N bond (around 286eV), indicating that molecules bound to the rGO surface through a nitrogen ligand are present in the outermost

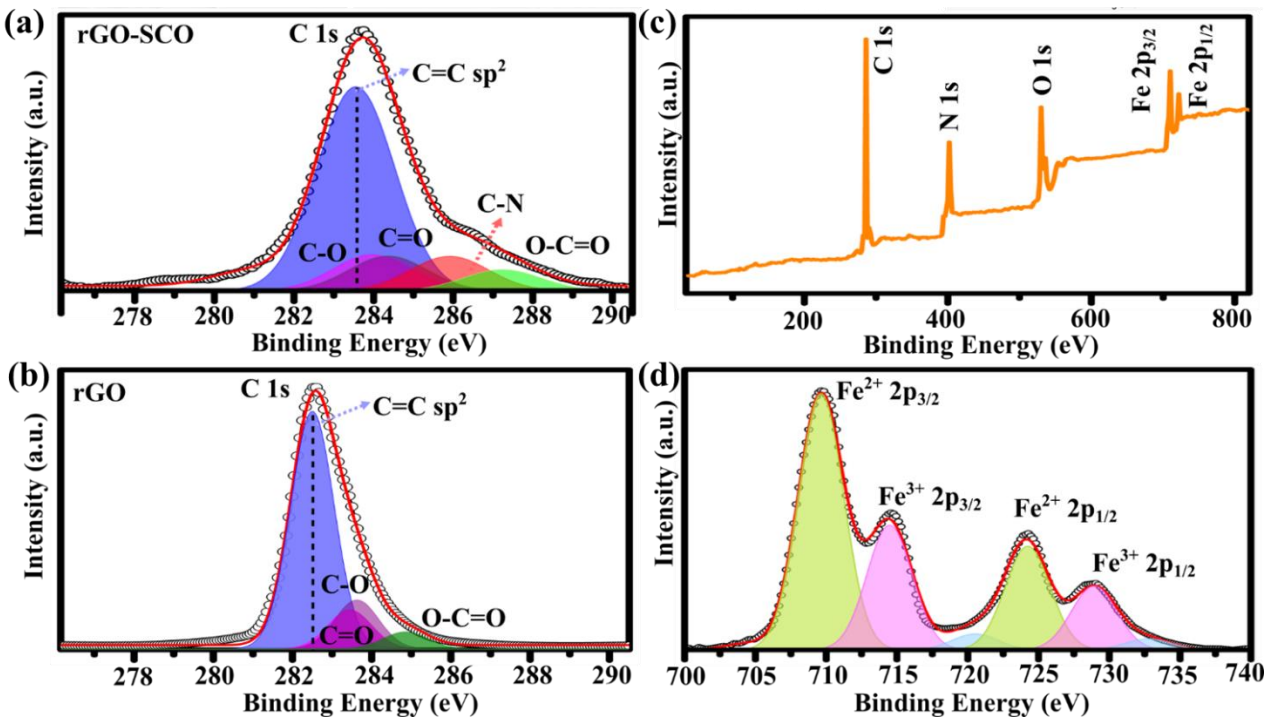


Figure 4.3. *(a), (b) High resolution C 1s XPS spectra of SCO-rGO composite and pure rGO respectively. Deconvolution shows different bonding states like C-N bonding (red) appears in the hybrid. Shift in the binding-energy with broadened FWHM due to charge transfer is observed in SCO-rGO heterostructure. (c) Overall XPS spectrum of the rGO-SCO composite (d) XPS spectra for the oxidation states of Fe in Fe-containing Triazole complex.*

part of the SCO structure. Conversely, in the pristine rGO C 1s spectra (**Figure 4.3b**), no such peak position was identified. The attachment of the SCO nanostructure caused a significant shift

in the most substantial C=C peak (originating from sp2 hybridized carbon atoms) towards a higher binding energy side. Specifically, the peak, initially at about 282.5 eV for rGO, shifted to 283.7 eV for the SCO-rGO nanocomposite. This change in binding energy signifies charge transfer between rGO and SCO nanostructures at the interface. Notably, after the attachment of SCO networks, the full width at half maximum (FWHM) of the C 1s spectra increased primarily due to the attachment of the triazole-based compound to the carbon surface. Upon deconvolution of the Fe 2p states (**Figure 4.3d**), we identified two oxidation states of Fe, characteristic of the Fe-containing Triazole compound. Peaks around 709.7 eV and 724.3 eV corresponded to Fe^{2+} $2p_{3/2}$ and $2p_{1/2}$ levels, while peaks at around 714.4 eV and 728.9 eV indicated Fe^{3+} levels. Two small additional peaks were observed as satellite spectra of the Fe 2p phase.

4.4 Electronic transport in SCO/Graphene and SCO/rGO hybrid system.

4.4.1 Electronic transport in SCO/Graphene hybrid system

In the context of the SCO/Graphene hybrid system, we conducted electrical transport measurements in a field effect geometry. These measurements took place within a dipstick, with the sample's temperature controlled by a Lakeshore temperature controller using a PT-100 temperature sensor positioned beside the sample. Measurements were done in four-terminal configuration using a lock-in amplifier (detailed in Chapter 2 section 2.3).

Prior to decorating the SCO molecule on the Graphene field-effect transistor (FET), we examined the Resistance (R) vs. Temperature (T) characteristics across the temperature range of 300 K to 400 K. The results revealed that with increasing temperature, the resistance of the Graphene sample exhibited a linear increment, indicating a metallic behavior, as illustrated in **Figure 4.4a**. Following the decoration of the SCO molecule using a simple drop-cast and spin-coating method, we conducted the R-T characteristics under identical conditions. The R-T measurement revealed a notable decrease in resistance at approximately 360 K during the heating cycle and a sharp increase in resistance around 334 K during the cooling cycle (**Figure 4.4b)**. The temperature at which the resistance changes in the Graphene channel aligned with the spin transition temperature previously reported for the SCO molecule, where the molecule goes to high spin (HS) state from

the low spin (LS) state during the heating cycle at around 360 K and at around 340 K it goes to low spin state from the high spin state. The observed hysteresis in the resistance change during the heating and cooling process suggests potential applications as a memory device, with a hysteresis width of approximately 26 K. It has been clear from the data that Graphene channel can clearly sense the change in spin state of the molecular system. The variation in Graphene resistance is

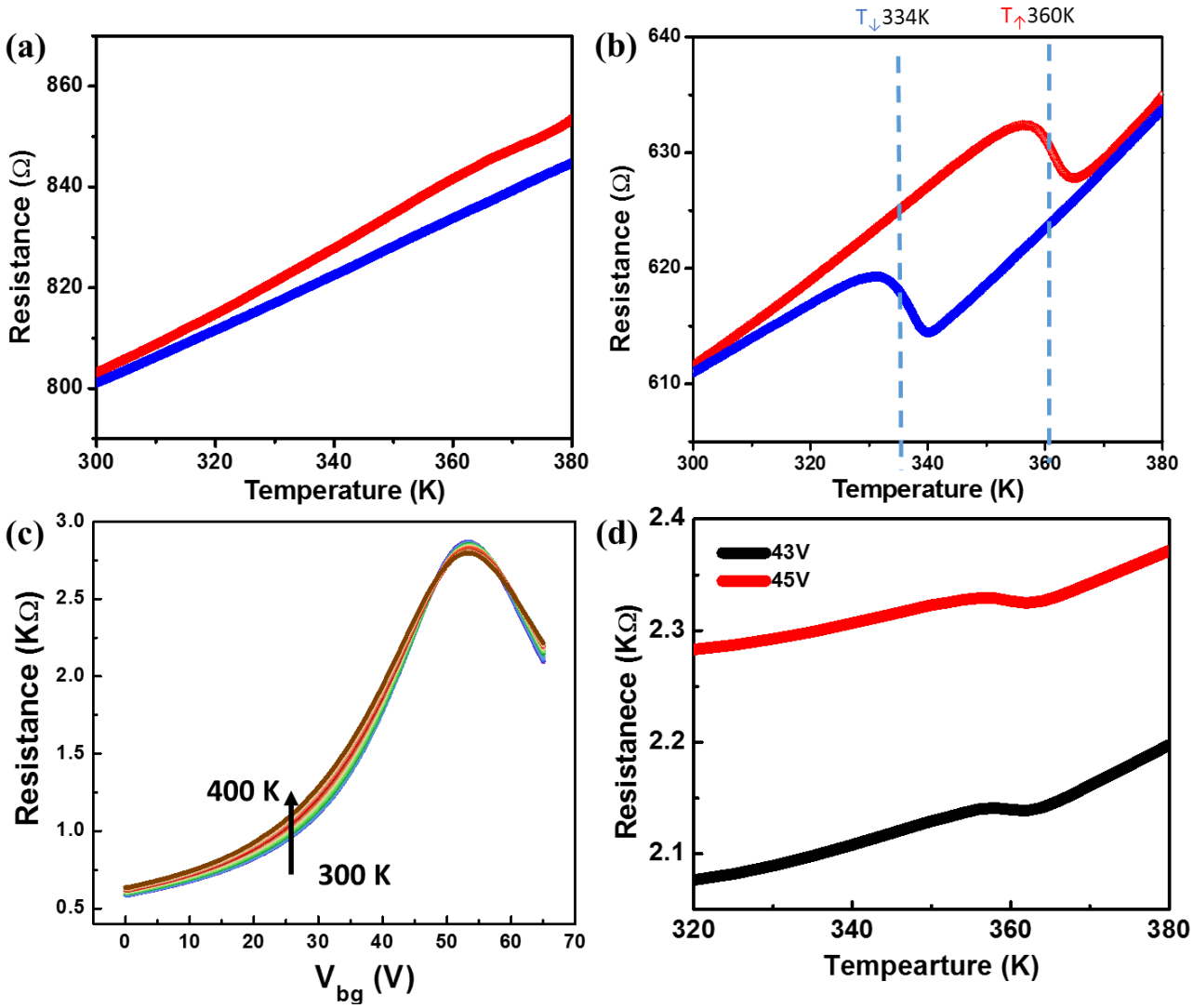


Figure 4.4. *(a) R-T characteristics of bare Graphene device showing linear increase in resistance during the heating and cooling cycle (b) R-T characteristics of a Graphene FET decorated with SCO molecule, showing a resistance change during the change in the spin state of the molecule. (c) R-V_{bg} characteristics SCO decorated Graphene device at various temperature. (d) R-T curve at various gate voltage extracted from the R-V_{bg} characteristics showing the sharpness of the change in the resistance can be tuned by the application of gate voltage.*

ascribed to alterations in the scattering contribution resulting from remote interfacial phonons originating from the spin state changes of SCO nanoparticles[21]. The structural transformations

during the spin state switching of SCO molecules induce a modification in the molecule's polarization state which couples with the interfacial phonon.

In our investigation, we conducted R-V_{bg} characteristics at various temperatures using the Graphene device decorated with SCO (Spin-Crossover) nanoparticles. The results, presented in **Figure 4.4c**, unveiled a noteworthy observation regarding the sensitivity of the device to spin transitions, particularly in response to variations in gate voltage.

The graphical representation in **Figure 4.4d** demonstrates that the modulation of spin transition sensing is achievable through manipulation of the gate voltage. Notably, within the gate voltage range of 20 V to 40 V on the R-V_{bg} curve, the change in resistance is notably more prominent compared to alterations observed at other gate voltage values. This suggests a distinct and heightened sensitivity to spin transitions in this specific gate voltage range. The observed correlation between gate voltage and the extent of resistance change underscores the potential for tailored control and optimization of spin transition sensing in the SCO-decorated Graphene device, offering valuable insights for device design and application in spintronics or sensor technologies.

4.4.2 Electronic transport in SCO/rGO hybrid system

In this investigation, we explore the conductance characteristics of hybrid composites comprising spin-crossover (SCO) and reduced Graphene oxide (rGO) under a thermal cycling regimen. **Figure 4.5a** illustrates the first cycle of low concentration (LC), wherein the heating mode induces a sharp low-spin (LS) to high-spin (HS) state transition at approximately $T_{1/2up}$ = 367 K, resulting in a substantial 136% reduction in conductance. Conversely, during the cooling mode, the reverse transition (HS to LS) occurs at around $T_{1/2down}$ = 341 K, accompanied by a notable 130% increase in conductance. The observed electrical hysteresis, characterized by two abrupt changes in conductance, is linked to the ON/Off state (1/0) with a high-memory channel, and the hysteresis loop width (ΔK) is measured at 26 K for LC.

For high concentration (HC) as depicted in **Figure 4.5b**, the LS to HS transition takes place at $T_{1/2up}$ = 393 K, resulting in a significant 112% decline in conductance. During the cooling mode, the reverse transition occurs at $T_{1/2down}$ = 375 K, accompanied by a 110% rise in conductance and a ΔK of 18 K. Despite hybridization with the 2D rGO template, each sample exhibits substantial thermal hysteresis, indicating the preservation of cooperativity even in the composite phase. Although the overall transport is mediated by the rGO surface, the conductivity is highly dependent on the spin state due to the presence of Fe(II) SCO centers.

The hysteresis width (ΔK) of LC is almost 60% higher than that of HC, unlike pristine SCO nanoparticles, where the typical hysteresis width decreases with the reduction in the volume of

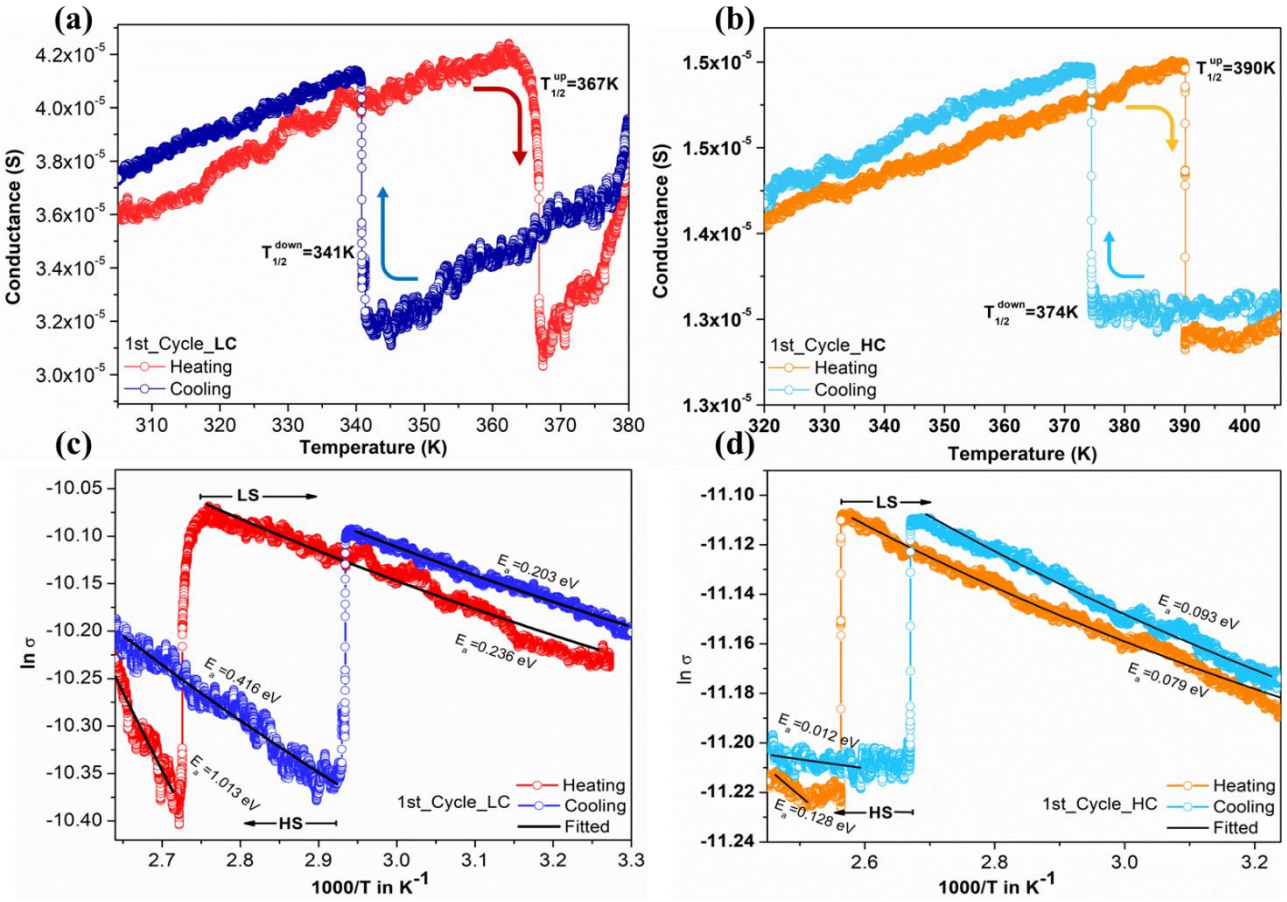


Figure 4.5. *Thermal cycling in conductance measurement, (a) 1st cycle of LC,(b) 1st cycle of HC, (c) Fitting of Arrhenius equation in the 1st cycle of LC, and (d) in the 1st cycles for HC.*

SCO. The surface-to-volume ratio increases significantly for LC, while for HC, the out-of-plane 3D growth potentially obscures the interfacial interaction with rGO. The broader hysteresis loop and the shift in transition temperature in LC may be attributed to charge transfer-induced interfacial

cooperativity enhancement and a variation in ΔE_{HL}^{0}, along with its inhomogeneous distribution. By confining the assembly of nanoparticles to the surface of rGO, the electrical pathway aligns preferentially along a specific plane, where the relative change in metal-ligand bond length is maximized during the LS/HS transition.

To regulate the dependency of spin state on electrical conductivity, we opt for a thermally activated process within the heterostructure, diverging from the tunneling mechanism proposed by Constantin et al. Despite the challenge in precisely identifying the hopping mechanism in the SCO-rGO hybrid due to the restricted temperature range and relatively modest changes in conductance, we employ the Arrhenius equation $\sigma_{dc}(T) = \sigma_0 exp(-E_a/k_B\,T)$ to gain a qualitative understanding of the variation in thermal activation energy during the LS/HS transition. Here, σ_0 denotes the pre-exponential factor, k_B is Boltzmann's constant, and E_a is the activation energy. Analysis of the temperature-dependent conductance data in **Figure 4.5c** and **Figure 4.5d** reveals a significant change in activation energy as the spin state transitions between LS and HS.

In the low concentration (LC) sample, during the first cycle, $\langle E^a_{LS} \rangle$ = 0.212 eV increases to 0.714 eV $\langle E^a_{HS} \rangle$ for the HS state. Conversely, in the high concentration (HC) sample during the first cycle, $\langle E^a_{LS} \rangle$ = 0.076 eV, and upon transitioning to the HS state, the average activation energy rises to $\langle E^a_{HS} \rangle$ = 0.239 eV.

Considering transport through a hopping mechanism, the change in dc conductance can be associated with modulation in hopping distance, with a hopping frequency corresponding to the relevant phonon frequency. In the HS state, the molecular structure of SCO relaxes, leading to an increase in metal-ligand bond length. This results in a shift in vibrational density of states to lower frequencies. Hence, the phonon contribution is more relevant in the LS state than the HS state, resulting in higher conductance in the LS state. . If we consider phonon frequency to couple the dc conductivity with the hopping frequency, Einstein's diffusion relation can be written following[151]:

$$\sigma_{dc} = \frac{n(el)^2}{6k_BT}\upsilon_P = \frac{n(el)^2}{6k_BT}\upsilon_{0_P}\, exp(-E_a/k_BT) \quad \text{.....(4.1)}$$

where n is the carried density, e is the charge, l is the hopping distance, ν_P is hopping frequency, ν_P is the phonon frequency and E_a is the activation energy[151]. Comparing this to the Arrhenius equation, we have found that the pre-exponential factor is basically consisted of hopping distance and hopping frequency. Thus, the observed conductance change is primarily related to the

competition between hopping distance and hopping frequency in the LS and HS states. In the HS state, the hopping distance is more considerable due to higher activation energy and in the LS state, hopping frequency is higher, in line with the previous reports[152].

4.5 Magnetic Measurement

4.5.1 Magnetic field induced excited spin state transition in the hybrid nanostructure

To understand the role of surface on the spin-state transition of the two separately prepared 2D SCO networks over the rGO surface, we have measured the dc mass susceptibility of pure Fe-Trz SCO and composite samples in a SQUID magnetometer (Quantum Design MPMS XL7) over the temperature range 240-400 K in the heating-cooling mode at a rate 3 K/min under different applied magnetic fields (0.2 T, 1 T, 3 T, and 5 T). **Figure 4.6a, c** compares the χT vs. T plots for HC and LC. At the lowest applied field of 2000 Oe (**Figure 4.6a,b**), a gradual spin transition occurs for HC with a narrow hysteresis loop, representing weak cooperativity among the spin-active Fe(II)-centers in the 2D assembly of nanoparticles. Surprisingly, as the magnitude of the field is increased (i.e., from 1T to 5T), the transition occurs more sharply, along with a notable shift in the spin transition temperature ($T_{1/2}$), leading to broader hysteresis loops. This effect is more prominent in case of LC rather than HC. For LC, the sharpness (*aka* abruptness) of the transition and the hysteresis loop width are more tunable than HC. From the derivative plot of χT vs. T (**Figure 4.6 b, d**), we estimate precisely the $T_{1/2}^{up}$ and $T_{1/2}^{down}$, representing the characteristics spin transition temperatures during LS to HS and HS to LS transition, respectively. Moreover, the mean transition temperature $<T_{1/2}>= (T_{1/2}^{up} + T_{1/2}^{down})/2$ shifts towards room temperature in the SCO-rGO composite phases (**Figure 4.6e**). While pure $[Fe(HTrz)_2(Trz)](BF_4)$ phase has $<T_{1/2}> =362$ K; it reduces to 337K and 323K for LC and HC, respectively. For estimation, the difference between spin transition temperatures $T_{1/2}^{up}$ and $T_{1/2}^{down}$, $\Delta T(K)$, is plotted as a function of B (**Figure 4.6f**). The maximum hysteresis width (ΔT) is ~26 K and ~62 K for HC and LC, respectively, whereas for pure Fe-Triazole nanostructures, it is ~39 K.

In the earlier studies on pristine SCO compounds, it was observed that transition temperature could only be shifted a little based on different parameters like nanoparticle shape/size, heating-cooling rate, ligand geometry and chemical variation, synthetic conditions, etc.; [29,30] albeit, remains invariant under the magnetic field. Here, firstly, the shift of the transition temperature towards

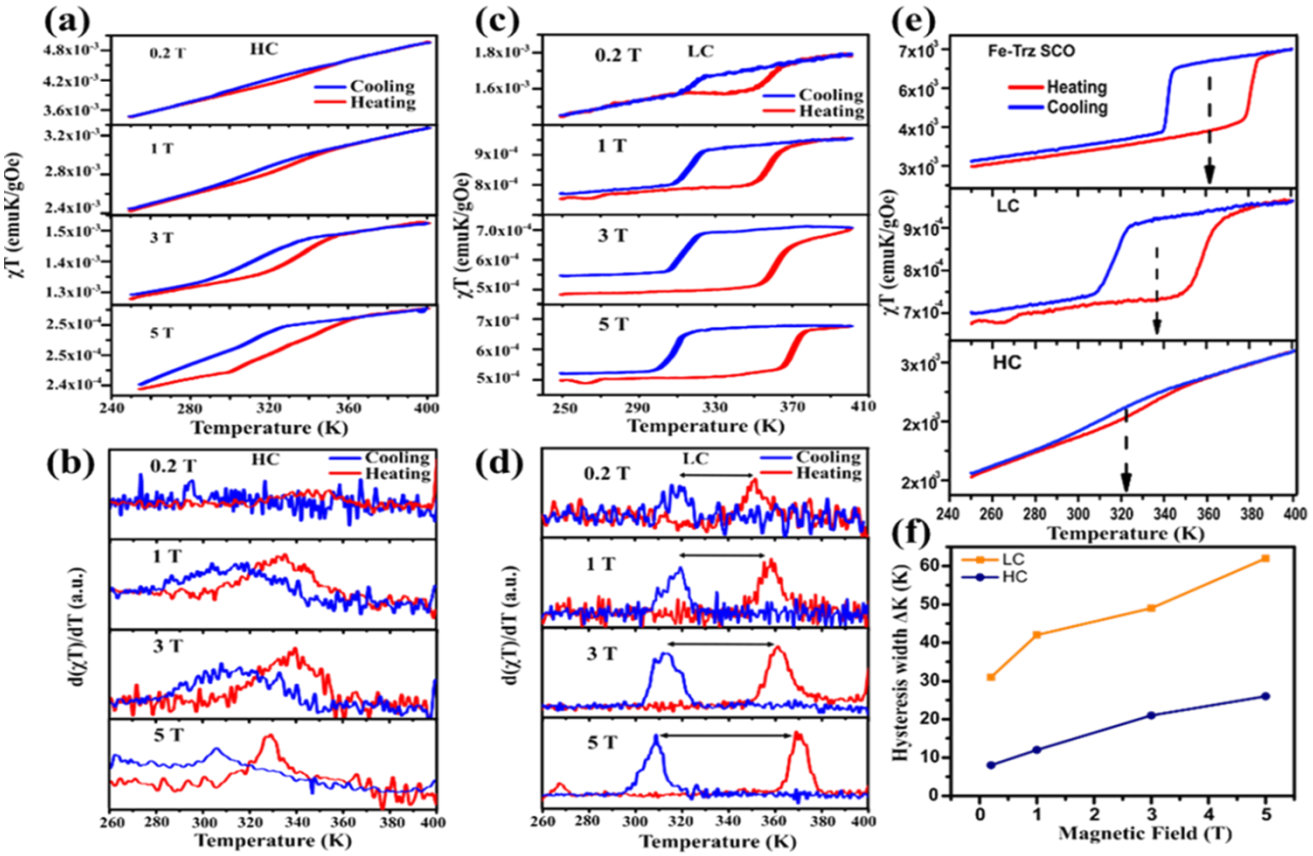


Figure 4.6. *(a), (c) χT vs. T plots for two different composites with varying concentration of SCO shows field induced cooperative effect. (b), (d) Corresponding derivative of χT plot shows the shift in spin transition temperature with enhanced interaction. (e) The variation of middle of hysteresis, for pure SCO NPs, and LC SCO-rGO and HC SCO-rGO composites is represented. (f) The variation of hysteresis width with magnetic field for different concentration SCO-rGO composites.*

lower temperature in the hybrid heterostructure essentially attributed to the magnetic-field induced thermodynamic stabilization of the Fe(II) HS state in the SCO nanostructures arises by reducing the zero-point energy difference (ΔE^0_{HL}, and its inhomogeneous distribution) towards negative values without sacrificing the cooperativity due to growth of SCO nanostructures on 2D rGO surface. Secondly, the enhanced sharpness of the hysteresis loops with the magnetic field indicates a field-induced spin-state transition. Finally, the broadening, as well as the sharpness of the hysteresis in the case of LC, further points towards the magnetic-field driven and the interface-

induced enhanced cooperativity among the spin-active Fe(II)-centers in the 2D assembly of nanoparticles of the SCO-rGO composites. Our calculations, discussed later, further indicate the strengthening of the intra-chain Fe-Fe antiferromagnetic (AFM) interaction in SCO-rGO composites due to creation of the additional superexchange pathways through rGO.

Although the cooperativity leading to thermal hysteresis is believed to be predominantly elastic in nature, the magnetic exchange interaction between Fe centers in the chain adds onto this effect. On the heating path, one starts with the LS state of the Fe centers, and thus has no associated magnetic energy. On the other hand, in the cooling path, the Fe centers are in HS state and HS (S=2) -> LS (S=0) transition amounts to loss of magnetic exchange energy between Fe centers. This additional effect, which is present in cooling path, and not in heating path making $T_{1/2}^{down}$ less than $T_{1/2}^{up}$.

4.5.2 Evolution of spontaneous magnetization in rGO/Fe-Trz nanocomposites:

To understand the possible role of magnetic interactions and distinguish the role of SCO nanoparticles, we measure the zero-field-cooled (ZFC) – field-cooled (FC) susceptibility of both pure rGO and the SCO-rGO nanocomposites (two different coverages) over the temperature range 2-400 K under 1T field at a heating-cooling rate of 3 K/min. For ZFC data, the sample was initially cooled till 2K and the heating data (2 K – 400 K) was recorded with an applied field of 1T. It is assumed that as there is no anisotropy, the FC heating/cooling curve will remain same. For rGO (**Figure 4.7a**), a typical defect-induced paramagnetic states can be observed at low temperatures with no bifurcation between ZFC-FC modes, similar to the earlier reports in chemically synthesized rGO[153]. When the Fe-TRZ SCO network is attached to the rGO surface (in the case of LC), χ-T plots exhibit additional noticeable bifurcations in the ZFC-FC curves at a lower

temperature region, away from the thermal spin crossover regime (**Figure 4.7b**), suggesting an exchange-induced effect in the hybrid.

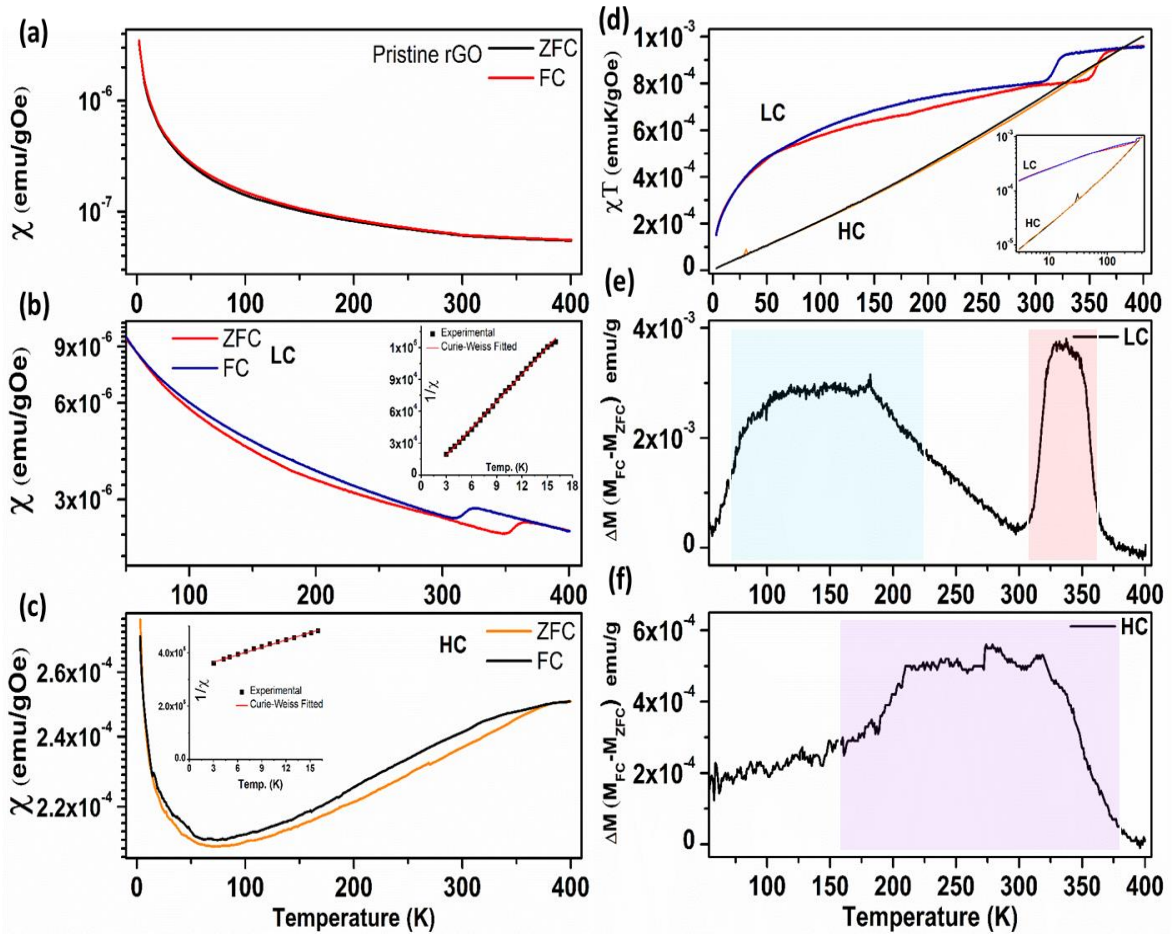


Figure 4.7. *Mass susceptibility vs.Temperature plot for (a) rGO, (b) LC SCO-rGO composite, (c) HC SCO-rGO composite. Inset of (b) and (c) show the 1/ χ vs. T plot for respective hybrid system. (d) χT vs. T plot for the two composite systems. Inset shows the log-log plot for χT vs. T plot. (e) and (f) show the differential magnetization plot for LC and HC SCO-rGO composite respectively.*

In HC (**Figure 4.7c**), similarly, a broad bifurcation with susceptibility rising with temperature in the low temperature range is evident. For further understanding of the magnetic interaction at low temperature, when 1/χ vs. T is fitted with the modified Curie-Weiss law: $\chi = C/(T-\theta)$, a negative θ value of -36 K is obtained for HC (**Inset Figure 4.7c**) implying the presence of AFM coupling. While for LC, θ comes out as positive (~0.82 K), suggesting a weak ferromagnetic (FM) interaction. To compare the strength of the FM and AFM coupling for two different SCO coverages on rGO, we have plotted χT vs. T for LC and HC in **Figure 4.7d**. For perfect antiferromagnets, when T→ 0 K, moment at 0 K should vanish. In this case, χT falls off more rapidly for HC than

LC (inset of **Figure 4.7d**) and reaches a magnitude of ~ 8.2×10^{-6} at 2 K, two orders of magnitude lower compared to LC (~1.5×10^{-4}). It can be concluded that the AFM ordering in case of HC is much stronger than LC, due to thicker volume fraction of SCO nanoparticles network, further confirmed by DFT calculation, which is discussed later. In ΔM vs. T plot (**Figure 4.7e,f**) for LC and HC, [$\Delta M = M_{FC}-M_{ZFC}$], only a single broadened peak (purple region) centered around 264 K is observed for HC, whereas LC exhibits two distinct peaks at 136 K (broad: blue region) and 335 K (sharp: red region). While the high-temperature peak (for LC) corresponds to the characteristic spin-crossover regime of Fe-Triazole phase, the additional low-temperature peak corresponds to magnetic ordering in the complex as a result of interfacial hybridization with 2D rGO. Appearance of bistable memory states in magnetization parameters:

To trace the enhanced magnetic coupling among the Fe(II)-SCO centers during LS/HS transition, we have thoroughly collected the MH loop of Fe-Trz SCO/rGO hybrid at different temperatures in both heating and cooling cycles. In both cases, truncated hysteresis loops without complete saturation are noticed, similar to the observations in granular magnetic systems. [154,155] For HC, during heating mode at temperatures 320 K, 340 K, and 380 K, the hysteresis loop is widened, and the area under the curve increases compared to its previous temperature state (**Figure 4.8a**). This is unusual for magnetic systems, as with the rise in the thermal energy, anisotropy decreases in a much faster rate than magnetization[156,157]. Quantitatively, the anomalous giant increment in coercivity and remnant magnetization with temperature are 95% (1439 Oe at 320K → 2815 Oe at 380 K) and 97%, respectively. This change is quite astonishing compared to pristine Fe-Trz SCO, where LS to HS trantion involves diamagnetic to paramagnetic phase change with zero coercivity[158]. Contrastingly, in SCO-2D hybrid, a giant coercive field (~2800 Oe) and high exchange bias predict the presence of both ferromagnetic and anti-ferromagnetic coupling in the hybrid. During cooling mode hysteresis from 340K to 280K, the loop quenched to its initial state as the HS state depopulated to the LS state (**Figure 4.8b**).

For LC, starting from 250 K, the MH loop shows a considerable coercivity (445 Oe) and remnant magnetization (0.007 emu/g). During the heating cycle from 320 K to 380 K, the hysteresis loop is also widened here with a better tendency to saturate (**Figure 4.8c**). At 380 K, a maximum coercivity of 1664 Oe has reached with the highest remnant magnetization (0.02 emu/g). Hence, almost a 274% increment in the coercive field and a 185% increment in remnant magnetization

have been observed in LC. During cooling from 340 K to 250 K, it is noticed that the decreasing trend in coercivity and remnant magnetization reversed as the high spin states start to depopulate (**Figure 4.8d**). In the inset of **Figure 4c,d** the schematic diagrams show a thin layer of SCO over rGO. To understand the dependency of magnetization with the applied field, we fit the initial growth curve with the Law of approach to saturation magnetization (LAS) which is also followed for typical magnetic systems[159]

$$M = M_s\left\{1 - \frac{a}{H} - \frac{b}{H^2}\right\}\chi H \quad \text{..... (4.2)}$$

where M_s is the saturation magnetization and a, b are different constants. The χH term refers to paramagnetism, and in some cases, it is found to be proportional to $H^{1/2}$ (i.e., our case)[160]. This term is added since the magnetization does not saturate completely due to presence of itinerant antiferromagnetic spins and consistent fitting is observed.

To arrest the newly evolved memory in magnetization parameters (due to bistability) in the spin states we plot coercivity and remnant magnetizations as a function of thermal cycle (**Figure 4.8 e,f**). The cyclic curves create a distinct hysteresis loop. The area under the loop in LC is larger than HC, suggesting stronger cooperativity among the Fe-centers. To check whether the enhanced ordering in the nanocomposite is due to defect-induced magnetism of rGO or not, we also compare the hysteresis of pristine rGO and SCO-rGO hybrid in the low-temperature range 2-50 K For pure rGO, an explicit diamagnetic nature is observed due to the absence of any order, while for the hybrid, the MH curves follow the Brillouin type dependence,[161] discarding the role of any defect-induced magnetism due to rGO. The magnitude of the moment also increases largely compared to pure rGO, which is due to the addition of Fe(II) SCO centers in the 2D matrix. Details are given in the supporting information.

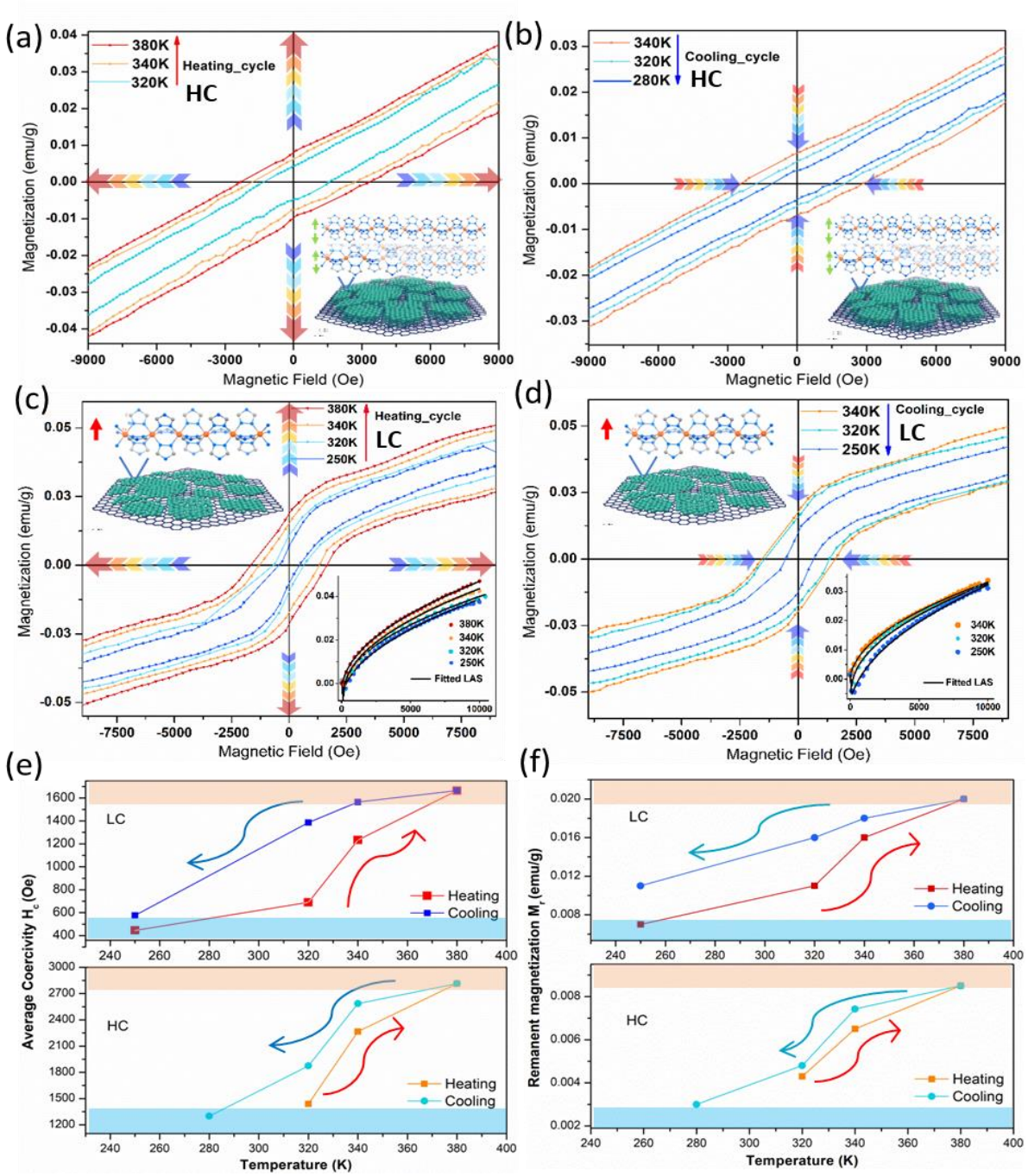


Figure 4.8. *(a) and (b): Heating and cooling cycles hysteresis loops for sample HC. (c) and (d): Heating and cooling cycles hysteresis loops for LC. Insets: the fitting with law of approach to saturation magnetization. Also, the LC and HC are represented schematically in the corresponding insets. (e) Comparison of bistability in coercivity variation in the two hybrid (f) Comparison of remanent magnetization variation in two hybrid systems.*

4.5.3 Molecular field approach for evaluating coupling constants:

In the SCO system, the nearest spins interact with Ising type spin Hamiltonian $H = -J_{ex,ij}S_i.S_j$. We have used molecular field approach to express the total susceptibility (χ_M as sum of three field components, two from the Fe HS/LS sites (H_{Fe}) and one from rGO interface (H_G). Field components (H_{ij}) are function of field coefficients (n_{ij}) and sublattice magnetization (M_{Fe}). While the field coefficients are governed by exchange coefficients $J_{ex,ij}$, the sublattice magnetizations have temperature dependence of Curie-Weiss type. After evaluating the mutual relationships among these parameters (see Supporting Information section 11 for calculation), ultimately exchange coupling constant J can be related to transition temperature T_c by the following relationship,

$$T_c = \frac{\left(J_{ex,Fe_{HS}G}\right)\left[Z_{Fe_{HS}G}Z_{GFe_{HS}}S_{Fe_{HS}}\left(S_{Fe_{HS}}+1\right).S_G(S_G+1)\right]^{1/2}}{3k_B} \quad \text{.....(4.3)}$$

Here S_i are the spin quantum number ($S_{Fe_{HS}} = 2, S_G = 1/2$), Z_{ij} is the number of nearest neighbours which is 2 in Fe-Trz SCO system. For HC, the transition temperature obtained during Curie-Weiss fitting has been used in this equation that gives a negative exchange constant: $\frac{J_{HC,Fe_{HS}G}}{k_B} = -25.4$. While, in the case of LC, this gives a weak positive exchange constant: $\frac{J_{LC,Fe_{HS}G}}{k_B} = 0.58$. Hence, the negative coupling constant of HC signifies antiferromagnetic interaction (anti-cooperative), while positive exchange coupling constant for LC represents weakly ferromagnetic type (cooperative) interaction. Their relative magnitudes indicate the strength of interaction among the hybrid system.

4.6 Discussion

Our findings illustrate that the creation of Fe-Trz-based spin-crossover (SCO) hybrids on 2D reduced Graphene oxide (rGO) not only preserves the desirable characteristics of both components—SCO and rGO—in each other's presence but also amplifies their properties through mutual assistance. This enhancement overcomes the hurdles for practical device applications. The designed device was thoroughly characterized using spectroscopic tools and first-principle calculations, revealing interfacial charge transfer between rGO and SCO.

Through careful manipulation of the rGO coverage area by SCO nanoparticle-networks, we achieved tunable magnetic properties. The susceptibility data at low temperatures indicates the prevalence of anti-ferromagnetic coupling in high-coverage samples, while low-coverage cases exhibit a weak ferromagnetic nature, suggesting an additional ferromagnetic interaction induced by the rGO/SCO interface.

Temperature-dependent hysteresis in the M-H curves, with a large coercive field around the spin-crossover regime at higher temperatures, confirms the presence of both antiferromagnetic intra-chain and ferromagnetic inter-chain interactions in the hybrid. Ab-initio calculations based on a simple model performed by Shladittya Karmakar from Prof. Tanusri Saha-Dasgupta's group further verify the enhancement of antiferromagnetic interaction between Fe centers via charge transfer with the conducting rGO substrate (not shown in this thesis). The ferromagnetic interaction may result from the emergence of a pinned magnetic moment in the conducting electrons of rGO, contributing to memory hysteresis with a large coercive field.

To measure the conductivity of the hybrid system, we fabricated micron-scale devices, revealing superior conductivity with bistability, showcasing potential for memory applications. In comparison to pristine SCO nanoparticles, the hybrid nanostructures exhibit enhanced cooperativity, improved conductance-bistability, and a variation in ΔE_{HL} with its inhomogeneous distribution, leading to a transition shift near room temperature for practical use.

The 2D rGO template provides a platform for stabilizing enhanced coupling in the spin centers of the SCO network. The interactions between SCO and the 2D substrate offer a mechanical and conducting backbone for the development of bistable nanoparticle-based hybrid devices.

4.7 Summary

- In this study, the goal was to functionalize Graphene-based materials, specifically CVD Graphene and rGO, to create a customizable memory device. The approach involved incorporating an electrically insulating SCO (spin crossover) molecule, capable of transitioning between low and high spin states under stimuli like temperature, light, or pressure. Devices were fabricated by attaching these SCO molecules to both CVD Graphene and reduced Graphene oxide (rGO).

- Electrical transport measurements demonstrated a direct correlation between spin crossover and temperature in both CVD Graphene and rGO-based devices. In the CVD Graphene-SCO hybrid, hysteresis was tunable by adjusting the gate voltage. Conversely, the rGO/SCO hybrid allowed for control over hysteresis width and transition temperature by varying molecular concentration.
- Magnetic measurements in the rGO/SCO heterostructure revealed that interfacial charge transfer-induced intermolecular interactions improved cooperativity. The hybrid exhibited both ferromagnetic (low coverage) and anti-ferromagnetic (dominant in high coverage) intra-chain interactions due to enhanced magnetic coupling, resulting in spontaneous magnetization states with a large coercive field. Overall, this research provides insights into the design and functionality of Graphene-based memory devices through the strategic integration of spin crossover molecules.

Chapter 5

Electronic transport and Low frequency noise in Tellurene FET

5.1 Introduction

Due to its exceptional linear energy dispersion and other special physical features resulting from its low dimensionality, Graphene has garnered a lot of attention in recent years[1,2,59,63,106]. However, Graphene's zero band gap restricts its use in semiconductor technology. Subsequently, layered transition metal dichalcogenides such as Molybdenum disulphide (MoS_2), Tungsten disulphide (WS_2) etc. were found to be semiconductors with larger bandgap[5,6,29,162,163]. This property led to an extremely high on/off ratio invoking their application as field effect transistors. Even though many semiconductors, especially TMDCs (such as MoS_2, WS_2, $MoSe_2$, etc.), have been thoroughly studied over the past decade, with orders of magnitude improvements in mobilities, the majority of these materials suffers from intrinsic defects or vacancies[5,6,20,36]. The synthesis of elemental semiconductors like black phosphorus[8,9,164,165] and the fabrication of FET devices with high mobility and ambipolar transport similar to Graphene are also being pursued, although these materials are unstable in ambient conditions.

Due to interfacial charge impurities and structural defects that are inherent to 2D semiconductors, a majority of them are n-type semiconductor[5,13,52,72]. Additionally, the Fermi level pinning at the metal/2D semiconductor interface, which leads to high Schottky barrier heights for hole injection, significantly impairs p-type conduction in most of the 2D semiconductors. For instance, MoS_2, one of the most researched 2D semiconductors, has a direct band gap of around 1.8 eV in its monolayer and an indirect band gap of about 1.2 eV in its bulk/multilayer forms. MoS_2 can be considered as intrinsically n-doped because the doping level of ultrathin MoS_2 layers is dominated by the environmental doping from the surface absorbents/supporting substrate and the electron doping from sulfur vacancies[5,6,27,28,36,162,166,167]. The family of p-type 2D semiconductors is, however, somewhat narrow, which restricts the widespread integration of 2D semiconductors in real-world uses. Many electrical and optoelectronic devices, including complementary logic circuits, phototransistors, and light-emitting diodes (LEDs), depend on p-type 2D semiconductors.

For instance, the complementary metal oxide semiconductor (CMOS) logic function in 2D electronics cannot be achieved without p-type conduction.

A promising option for future electronics is few-layer black phosphorus (FLBP)[42], which was separated from its bulk in 2014. It has excellent mobility, optical linear dichroism, moderate electronic and direct optical bandgaps, and other exceptional characteristics that bridge the gap between Graphene and transition metal dichalcogenides (TMDs)[42,168–173]. However, in ambient conditions, it is chemically unstable. Following that, recently, a new 2D elemental semiconductor, Tellurene[10,174–177], has been discovered in the hunt for high mobility and stable semiconductors. This is a monolayer-exfoliable van der Waal semiconductor with a narrow band gap (0.3–0.7 eV). Initial transport measurements show that few layer Tellurene based devices exhibit ambipolar behavior with a reasonably high mobility of ~ 200 cm^2/Vs, similar to Black Phosphorus but with better stability[178,179]. Being a narrow band gap semiconductor, Tellurene has shown also promises towards optoelectronic devices in the NIR regime[180,181] as well as for thermoelectric applications[182–184]. Apart from its applicability in electronic devices, various interesting physical phenomena like quantum hall effect[175], topological field effect transistor[11,185] or, observation of Weyl physics[11] have already been reported in this materials, making it a fundamentally interesting material. .

Here, we have synthesized few-layer Tellurene using hydrothermal method and fabricated field effect devices which clearly show ambipolar characteristics with I_{on}/I_{off} ratio, exceeding more than ~ 10^2 at room temperature and ~10^4 at low temperature. Study of 1/f noise in this device reveals, noise primarily arises due to the mobility fluctuation from the intrinsic defects. We also explore temperature dependent transport where we observe a metal to insulator like transition possibly occurring due to change in phonon and impurity scattering similar to conventional semiconductors like Si or Ge.

5.2 Synthesis of Tellurene using hydrothermal method

A typical technique[10,185,186] involves dissolving 1.5 g of poly(vinylpyrrolidone) (PVP) in 16 mL of DI water first, followed by the addition and dissolution of 46 mg of sodium telluride (Na_2TeO_3) to create a transparent solution. The aforementioned solution was then sequentially mixed with 1.66

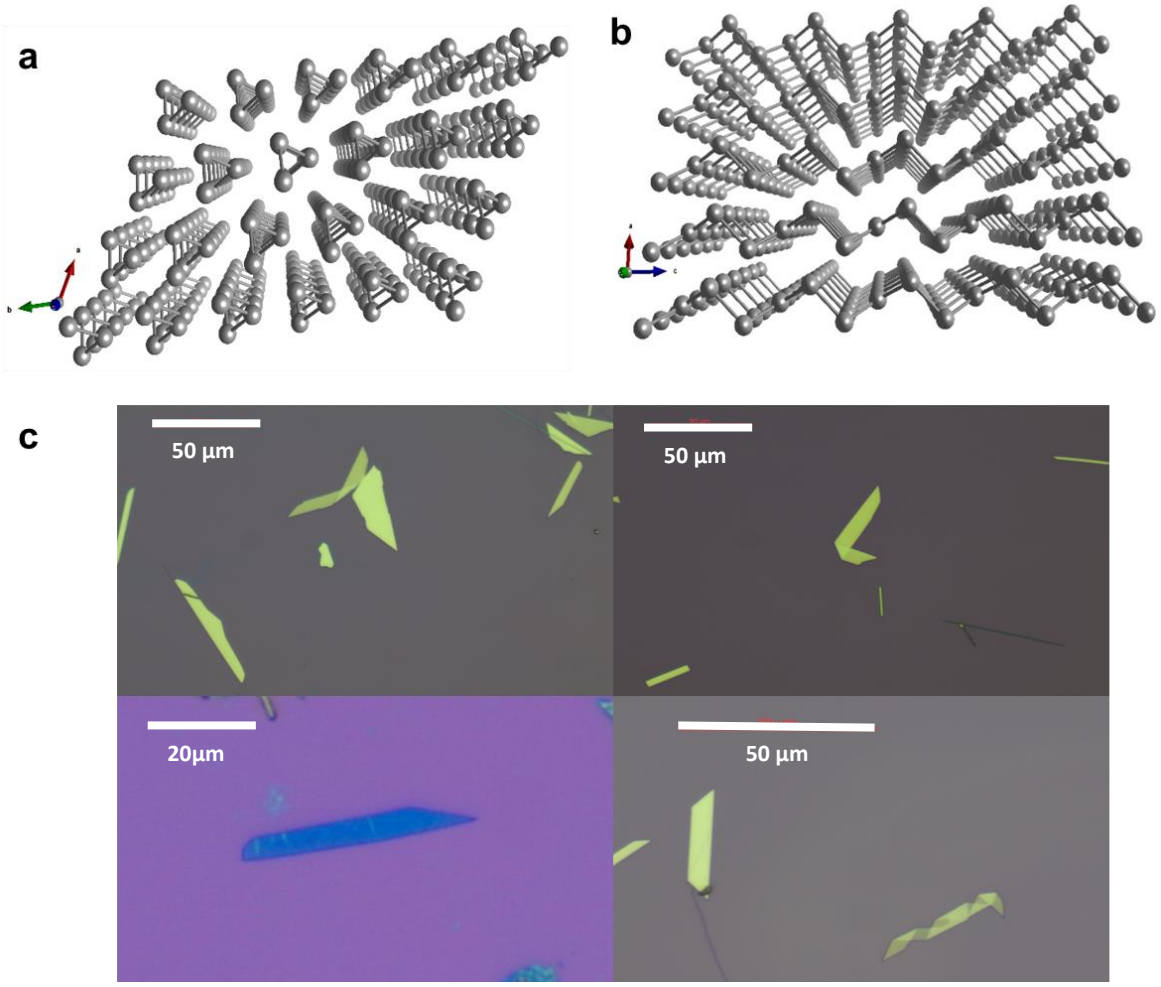


Figure 5.1. *Crystal structure of Tellurene (a) viewed from z crystal axis, (b) viewed from y crystal axis. (c) Optical image of the synthesized Tellurene.*

mL of ammonium hydroxide solution and 0.838 mL of hydrazine monohydrate. The solution was then poured into a 25 mL Teflon-lined stainless-steel autoclave. After being completely sealed, the autoclave was put inside of an oven. With a ramp rate of 3 °C/min, the autoclave was heated to 180 °C from room temperature and kept there for 4 hours. The autoclave was then taken out of the oven and quickly brought up to room temperature using running water. The finished product was centrifuged at 3000 rpm for two minutes to purify it and wash it three times with DI water. The finished tellurium solution is a silver-gray color after washing and purification. Tellurium nanoflakes with typical thicknesses in the range of 10–30 nm and typical lateral dimensions in the range of 10–50 µm are produced by maintaining the autoclave in an oven at 180 °C for 4 hours. It is crucial to note that altering the reaction time (4–30 h) at 180 °C can roughly adjust the thickness of tellurium nanoflakes. By extending the reaction, the thickness of the tellurium nanoflakes can

be increased. The final product was redispersed in pure ethanol before being transferred to the target substrate for characterization and device fabrication by drop-casting.

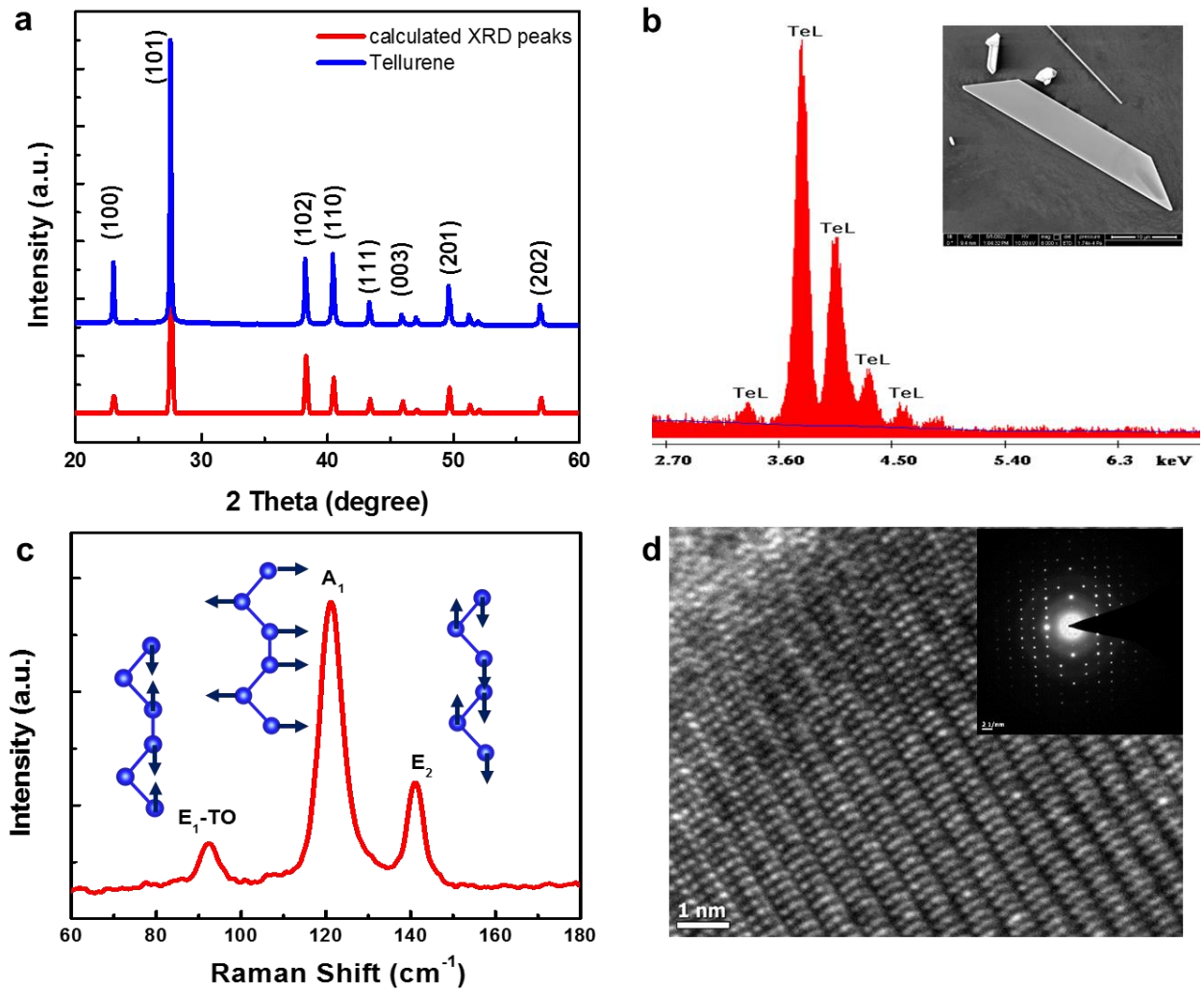


Figure 5.2 *(a) XRD pattern of the dried Tellurene flakes. (b) EDX spectrum of the prepared Tellurene flakes. (Inset) Scanning electron microscope image of the Tellurene flake. (c) Raman spectra of a Tellurene flake showing the three characteristics peak. (d) TEM image of the Tellurene flakes confirms the chain like structure of Tellurene. (Inset) shows the SAED pattern*

5.3 Crystal structure and Characterization

The atomic triangular helix chains of Te are stacked together in a hexagonal array, where the Te atoms are covalently bonded with their neighboring Te atoms in a helical chain (**Figure 5.1a, b**). In principle, Te is a true 1D system rather than a 2D van der Waals material. The zigzag layers can

be seen to be stacked together via van der Waals forces to form a 2D/3D structure when viewed from y axis. The X-ray diffraction (XRD) patterns of the synthesized Te flakes (**Figure 5.2a**) Prominent peaks located at 23°, 27.6°, 38.3°, 40.4°, 43.3°, 45.8°, 49.6°, 56.9°, and 63.8°, which correspond to the (100), (101), (102), (110), (111), (003), (201), and (202) planes in the hexagonal Te structure, respectively. The full-width-half-maximums of the main peaks were narrow, indicating that a high-quality Te structure was attained[10]. The EDX spectra shows the characteristic Te spectrum and no other peaks are observed which signifies the high purity of the sample. The as synthesized tellurene flakes are drop-casted in silicon wafer and characterized by SEM (**Figure 5.2b (inset)**) and optical microscope (as shown in **Figure 5.1c**.). The Raman spectra of 2D tellurene exhibits mainly three characteristics Raman active modes[10,181,187,188] at 92 cm^{-1} (E_1-TO), 121 cm^{-1} (A_1) and at 141 cm^{-1} (E_2) as shown in **Figure 5.2c**. These correspond to one A-mode (A_1) which corresponds to chain expansion in basal plane, and two E-modes (E_1 and E_2) bending of bonds along the chain direction (as shown schematically in **Figure 5.2c**). The sample is further characterized by High resolution TEM and selected area diffraction pattern (**Figure 5.2d and inset)** clearly displaying the chain like arrangement of the tellurium atoms with high crystallinity.

5.4 Experimental Details

5.4.1 Conductivity Measurement

Electrical contacts are defined using optical lithography using positive photo resist followed by evaporation of Cr/Au (5nm/60nm) metal and lift off. The optical micrograph of the fabricated device is shown in **Figure 5.3a**. The devices are then bonded and transferred to a dipstick where they are annealed at a temperature 400 K for 4 hours in a high vacuum of 10^{-5} mbar. It helps to get rid of unwanted adsorbents such as water molecule and lithographic residues to improve device performance. In all the devices the heavily doped silicon acts as a global back gate. Measurements were carried out in two probe configurations, using both lock in based low frequency ac and dc techniques. **Figure 5.3c-d** show the Current (I_{ds}) – Voltage (V_{ds}) characteristics of Device 1 at both 300 K and 77 K, respectively, measured with a Source measuring unit (Keithley 2450). The device exhibits ambipolar behavior. At both room temperature and 77 K, for $|Vds| \leq 500mV$ the I_{ds}-V_{ds} characteristics at all –ve gate voltages are almost linear and symmetric with a dominant p-type

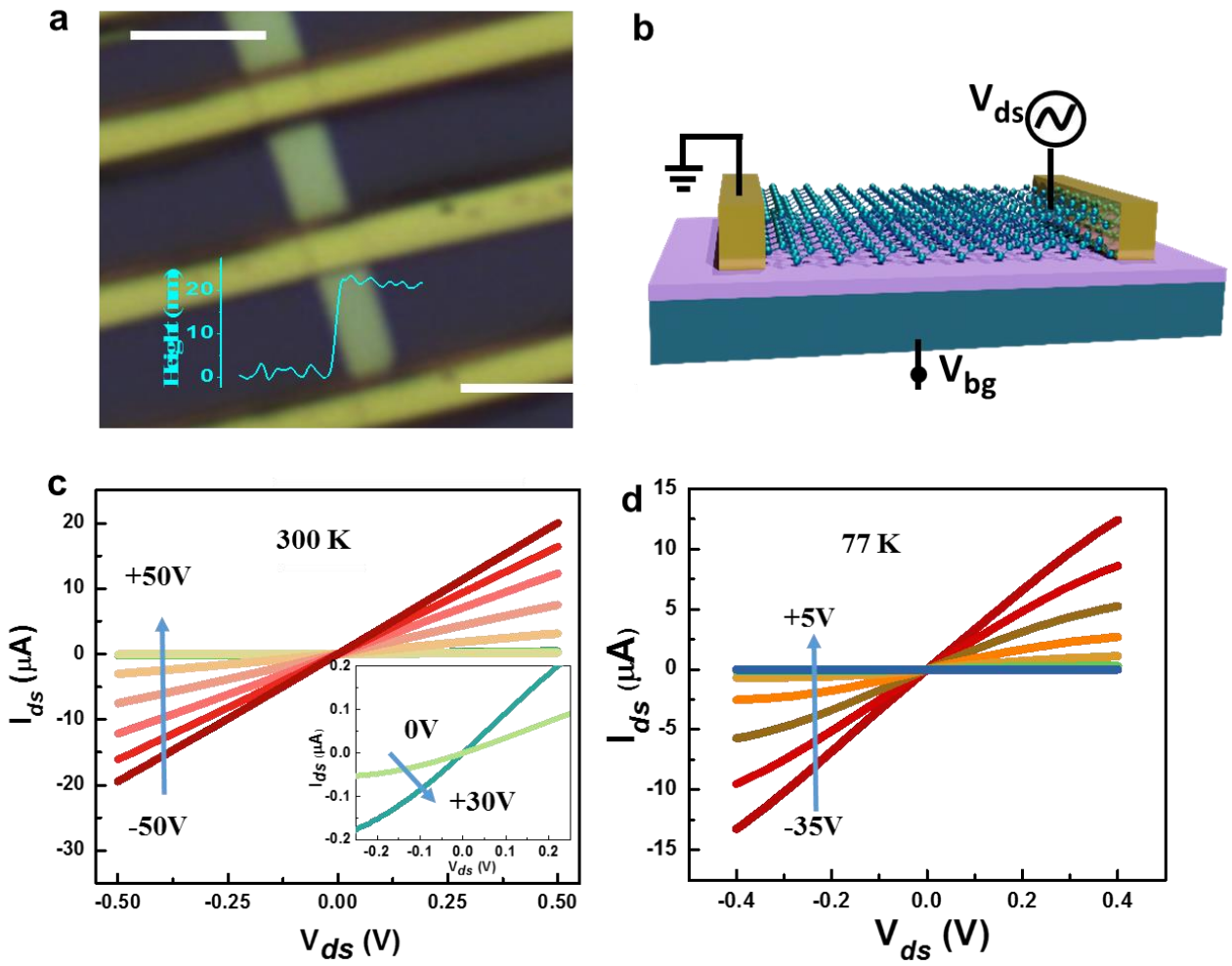


Figure 5.3. *(a) Optical micrograph image of the Tellurene device (scale bar 10 μm). (b) Schematic of the Tellurene FET. (c) I-V characteristics of a Tellurene FET with Cr/Au contact at 300 K shows a linear behavior at all –Ve gate voltage and shows a non-linear behavior at high +Ve gate voltage with low current, implementing a P type behavior. (d) At low temperature (77K) the device I-V characteristics shows a non-linear behavior at high bias condition at all gate voltages.*

behavior similar to recent reports[10,178,186]. At high +ve gate voltages the I_{ds}-V_{ds} characteristics reverse and shows a nonlinear behavior and low electrical current. Since we could not apply a large positive gate voltage beyond ~ 40 V, the chemical potential primarily resides close to the gap region and due to the presence of a small but finite Schottky barrier (will be calculated later), I_{ds}-V_{ds} characteristics show nonlinear behavior in the positive side. To gain better understanding, we sweep the gate voltage in both directions. **Figure 5.4a** show the transfer characteristics of the device for two difference bias (20 mV and 75 mV). Such a ambipolar characteristics was observed before in Tellurene devices[10,187]. In the region of moderate negative gate voltage, the holes are dominating the transfer characteristics and the device shows p type behavior. In the region of high

positive gate voltages electrons became the dominant charge carriers for the transport. With the change in the carrier type with the gate-voltage the device shows a p-branch enhanced ambipolar characteristics as shown in **Figure 5.4a**. The ambipolar transport is observed in varied source drain bias as shown in **Figure 5.4a.** In the hole side the increase in the I_{sd} with gate voltage is much steeper than the electron side, indicating a higher mobility than that of electron side. The larger current at the negative gate voltage could be due to higher density of states at the hole side, although the efficiency of the hole and electron injection into the Tellurene from the metal contacts may also be a significant factor. The calculated I_{on}/I_{off} ratio at room temperature is found to be of the order of ~ 1.5 x 10^2 which is little lower for any electronic on/off switches. The high dark current is possibly due to the combined effects due to materials defects, metal/semiconductor interface and lower bandgap and thickness of the materials and needs further improvement.

To estimate the contact resistance of the device, we have used the Y-function method. The Y-

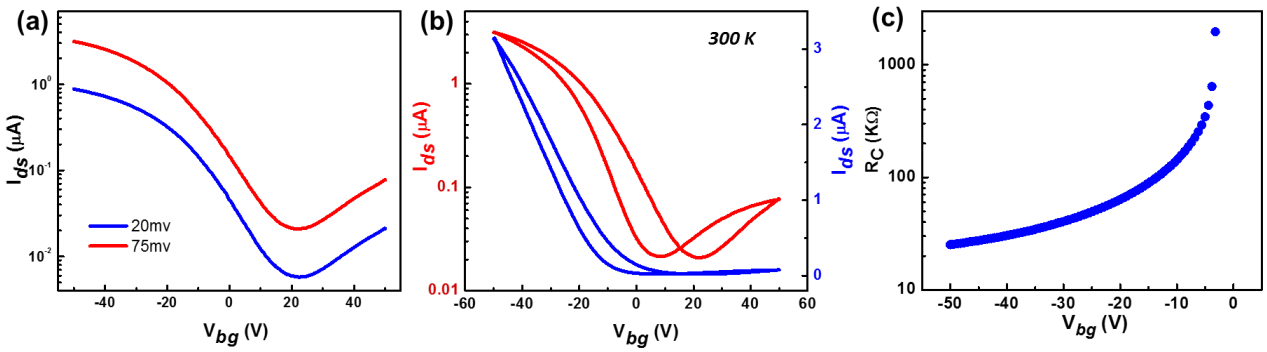


Figure 5.4. *(a) I_d vs V_{bg} characteristics at different drain source bias (b) I_{ds} vs V_{bg} characteristics at 75mv bias showing an ambipolar characteristics and hysteresis with the direction of gate-voltage sweep (c) shows the contact resistance calculated from the Y-function method.*

function method is a common method to calculate the contact resistance (R_C) of a 2D semiconducting system used instead of TLM method[178].

According to Y-function method the drain current can be expressed as[178,189]

$$I_d = \frac{W}{L} C_{ox}(V_g - V_T) \frac{\mu_0}{1 + \theta(V_g - V_T)} V_{ds}$$

$$\beta = \mu_0 C_{ox} \frac{W}{L}$$

Where I_d, V_{ds}, C_{ox}, are the drain current, drain bias, oxide capacitance accordingly. W and L are the width and length of the sample.

The channel mobility degradation factor (θ) can be expressed as

$$\theta = \theta_0 + \mu_0 C_{ox} \frac{W}{L} R_C = \theta_0 + \beta R_C$$

where θ_0 is intrinsic degradation coefficient of mobility, and it is very small that it can be ignored under normal condition. Therefore, we should only consider effect of R_C on degradation of mobility.

The Y-function is defined as

$$Y = \frac{I_d}{\sqrt{g_m}} = \sqrt{\beta V_d}(V_g - V_T)$$

$$g_m = \frac{dI_d}{dV_g} = \beta \frac{V_d}{[1 + \theta(V_g - V_T)^2]}$$

Where g_m is the transconductance.

Combining the above equation the contact resistance can be calculated using the following formula,

$$R_C = \frac{\theta}{\beta} = \frac{V_d}{I_d} - \frac{1}{\beta(V_g - V_T)}$$

Figure 5.4c shows the variation of R_c as function of gate voltage. At high carrier density the contact resistance starts to saturate and in the subthreshold region the Rc increases exponentially. From the saturation region at the on state we can estimate the R_c to be 25 kΩ which is comparable to reported cases in Tellurene device[178] and is much lower as compared to Ti/Au contacted MoS_2 FET's[190].

The sweep direction dependent I_d –V_{bg} characteristics of the Tellurene field effect transistor shows a significant hysteresis in the transfer characteristics, as shown in **Figure 5.4b**. The threshold voltage (V_{th}) at the hole side occurs at a gate voltage ~ – 3V when the gate voltage is swept from positive to negative side and at -17 V when the direction is reversed, leading to a change in threshold voltage (ΔV_{th} = 14V). Hysteresis in 2D materials based FETs are rather common at ambient condition as studied earlier, like on MoS_2, Graphene[191,192]. Two main causes of the hysteresis are due to the adsorbed water and oxygen molecule, or the trap states present in the SiO_2 channel which captures electrons from the channel. As we have vacuum annealed the sample and measurement were carried out in high vacuum, the presence of adsorbents can be ruled out. This suggests that the primary reason for hysteresis in the transfer characteristics is mainly due to the presence of interfacial oxide traps at the tellurene/ SiO_2 interface. The field effect mobility (μ_{FE})

of the device was calculated from the transfer characteristics using the relation $\mu_{FE} = L/(WC_{ox}V_{ds})g_m$, where W and L are the width and length of the channel, C_{ox} is the gate oxide capacitance per unit area of 300 nm SiO_2; and g_m is the transconductance. The calculated hole mobility is ~ 242.5 $cm^2 V^{-1} s^{-1}$ at room temperature, being in the similar range of the previous reports on back-gated Tellurene field effect transistors[177,181].

5.4.2 Temperature dependent electrical transport in Tellurene FET

To understand the charge transport mechanism further, we have measured the temperature dependent electronic transport inside a dipstick at high vacuum. The temperature was stabilized using temperature controller (Lakeshore, model 340). **Figure 5.5a** compares the drain transfer characteristics at 300 K and at 86 K. Firstly, the hysteresis almost vanishes at low temperature as the carriers do not get enough thermal energy for trapping detrapping processes. Secondly, the off current reduces below 1 nA, increasing the on/off ratio to ~10^4 compared to the room temperature value of ~10^2. This is attributed to a broader range of energy levels contributing to carrier conduction within the channel of the device. Consequently, the electron and hole branches, representing the energy levels of electrons and holes in the semiconductor, start to overlap to a greater extent. This overlap leads to an increase in the current (I_{ds}) even at the minimum gate voltage where the branches intersect. In practical terms, this means that the device begins to conduct more at the point where it should ideally be in the 'off' state due to the increased thermal energy. As a result, the on/off ratio, which is the ratio of current when the device is in the 'on' state to the current when it's in the 'off' state, decreases.

Figure 5.5b systematically plots the I_{ds} -V_{bg} characteristics (sweeping positive to negative V_{bg}) at different temperatures. It can be observed that the gate voltage associated with the minimum I_{ds}, denoted as V_{min}, shifts towards larger positive values, indicating an overall negative change in the charge contribution from traps. This phenomenon can be attributed to an increased occupancy of acceptor-like traps. At higher temperatures, a greater number of electrons can be captured, especially under the initial condition of the sweep with a substantial positive V_{bg} bias.

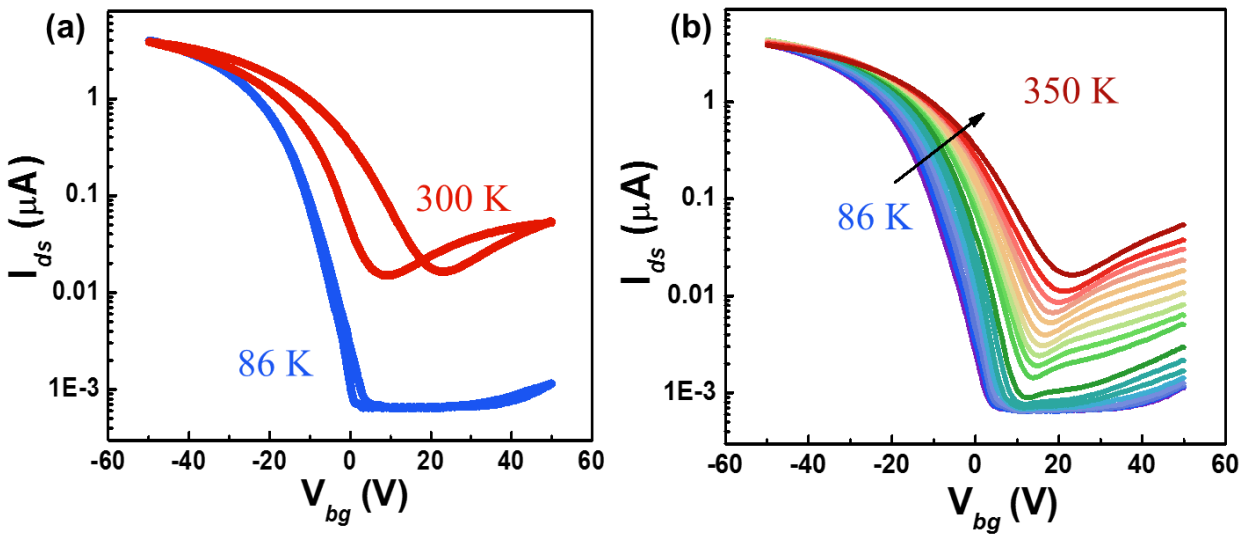


Figure 5.5. *(a) Dual gate sweep of transfer characteristics (I_{ds}-V_{bg}) of the Tellurene FET taken at 300 K and 86 K, showing enhanced hysteresis in the transfer characteristics at high temperature. (b) I_{ds}-V_{bg} in semi-log scale showing ambipolar characteristics at different temperature from 350 K to 86 K.*

Subthreshold swing, often represented as SS, stands as a pivotal parameter in the functioning of a field-effect transistor (FET). It gauges how effectively a transistor can do the transition between its ON and OFF states, particularly in the subthreshold operational region. To be precise, subthreshold swing is quantified as the alteration in the gate-source voltage (ΔV_{gs}) required to modify the drain current (I_{ds}) by a factor of 10. This relation can be mathematically expressed as –

$$ss = \frac{1}{\frac{\delta(log_{10}(I_{ds}))}{\delta(V_{gs})}}$$

At room temperature the SS is about 9.7 V/dec, the high value of SS can be attributed to the large thickness of the Tellurene flake and also presence of interfacial trap states near the semiconductor's band edges in the Tellurene flakes[42,193]. These trap states can capture and release charge carriers, causing non-ideal behavior in the transistor. Also, the quality of the dielectric material used in the transistor plays a crucial role. If there are defects or impurities at the interface between the semiconductor and dielectric, it can lead to a higher subthreshold swing. At low temperature (86 K) the SS reduced to 6.8 V/dec. At lower temperatures, the reduced thermal energy of charge

carriers leads to fewer carriers being excited into higher energy states and reduction of phonons reduces the scattering of charge carriers. This results in a more distinct transition between ON and OFF states, causing a decrease in subthreshold swing.

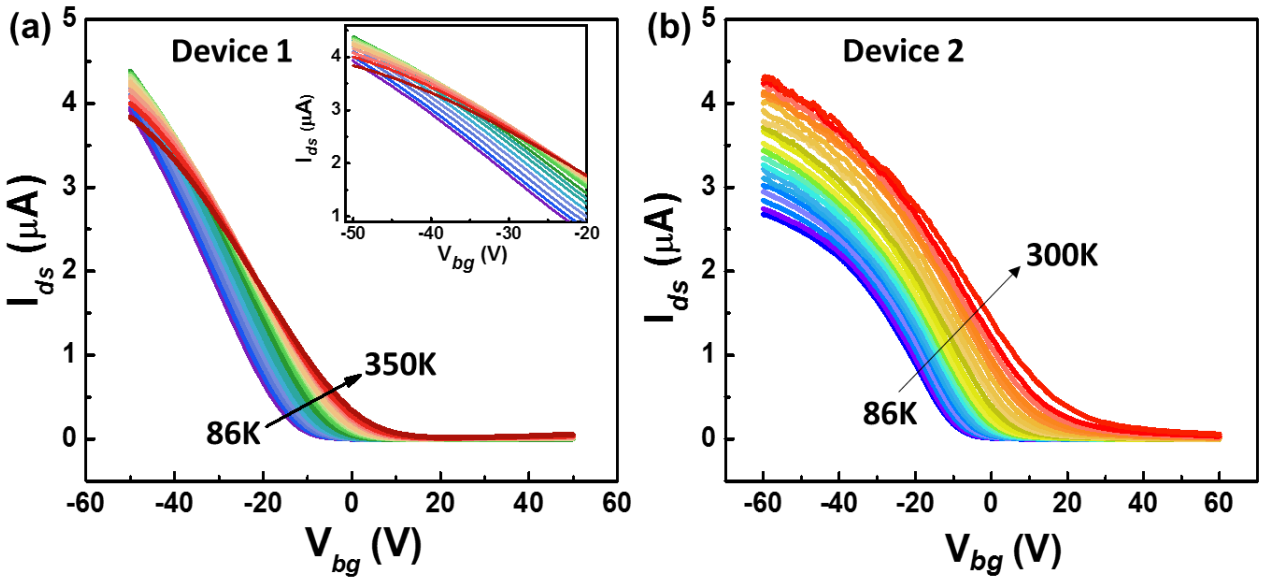


Figure 5.6. *Mobility dependent transport in Tellurene devices (a) Id-V_{bg} curve of a Tellurene FET having mobility of around 232 cm^2/Vs, shows a Metal to Insulator transition at moderate –ve gate voltage. (Inset) shows a closer view of the MIT. (b) Id-V_{bg} characteristics of device 2 with a low mobility of 24 cm^2/Vs behaves normally like a semiconductor with variation of temperature.*

We conducted electrical transport measurements on a range of devices, each with distinct charge carrier mobilities. Temperature dependence of two characteristics devices (Device 1 and Device 2) are shown in **Figure 5.6** having room temperature hole mobilities 232 cm^2/Vs and 24 cm^2/Vs respectively. Device 1, exhibiting ambipolar behavior with a mobility of 242 cm^2/Vs, demonstrated a noteworthy I_{ON}/I_{OFF} ratio. At room temperature, this ratio was on the order of 10^2, rising to 10^4 at lower temperatures. Upon varying the temperature in Device 1, a decline in current was observed after reaching 220 K, particularly at higher negative gate voltages (beyond -23 V), indicating characteristics reminiscent of a metal. At gate voltages below -23 V, Device 1 exhibited behavior akin to a conventional semiconductor. Here, conductance diminishes with decreasing temperature. In Device 2, the current increases all over the gate voltage region with increasing temperature, behaving like a conventional semiconductor.

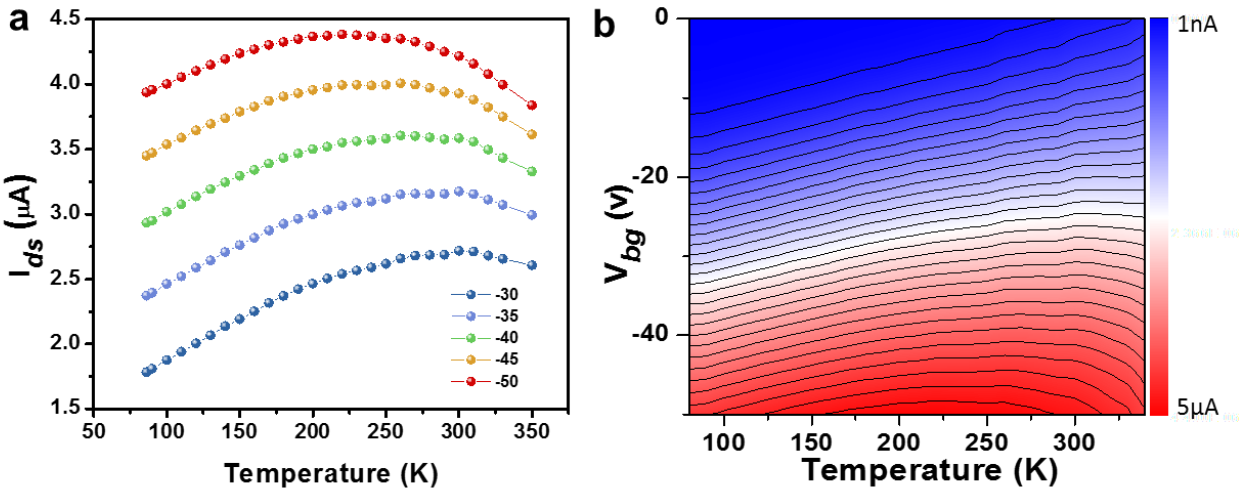


Figure 5.7. *(a) I_{ds} vs T curve at fixed negative gate voltage showing a metal to insulator transition at higher negative gale voltage. shown for Device 1(b) Variation of current at different gate voltages with temperature.*

For Device 1, **Figure 5.7a**, illustrates that as the gate voltage increases on the negative side (indicating a rise in gate-induced carrier density), the metal to insulator transition point shifts towards lower temperatures. **Figure 5.7b** presents the comprehensive trend of drain current at various gate voltages with respect to temperature. Notably, a discernible white line marks the metal to insulator transition point. The variation of color from blue to red indicates an increase of current.

Table 1. List of different Tellurene devices measured with their thickness, I_{on}/I_{off} ratio, mobility

Thickness (nm)	I_{on}/I_{off} ratio	Mobility μ (cm^2/Vs)
10	3×10^4	8
15	2×10^5	36
20	1×10^3	242
40	6.6×10^1	46
50	5.6×10^1	30

5.5 Schottky barrier and Mobility

As highlighted by Das et al[194]., the critical factor that hampers the performance of devices built with low-dimensional materials: the interface between the metal and semiconductor. This interface significantly constrains the device's overall capabilities. Consequently, gaining a deep understanding of how it affects carrier transport is essential when examining Schottky Barrier (SB)

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) that utilize two-dimensional (2D) channels. To determine the Schottky Barrier (SB) heights, one can employ a temperature-dependent investigation of two key processes: thermionic emission and thermally assisted tunneling. This analytical approach allows for precise extraction of SB heights, providing crucial insights into the behavior and performance of semiconductor devices with low-dimensional materials.

An approach to calculate the Schottky barrier height of a 2D FET using Landauer's formalism is given by Ivan et.al[195], where they have provided a closed-form expression for the current resulting from thermionic emission over the barrier at the interface between metals and 2D channels. The derivation commences with the Landauer equation, which describes hole conduction in the valence band of Te FET, and is represented as:

$$I = \frac{2q}{h}\int_{-\infty}^{E_V} T(E)M(E)[f_S - f_d]dE$$

Where *h* is the Planck's constant, *q* is the electronic charge, *T(E)* and *M(E)* are the transmission coefficient and density of modes respectively f_s and f_d are Fermi functions at the source and drain respectively. For small drain source bias (V_{ds}) we can approximate $f_s - f_d \approx -qV_{ds}(\frac{\partial f_0}{\partial E})$, and under Boltzmann approximation $\partial f_0/\partial E \approx (1/k_BT)\exp[(E - E_{F0})/(k_BT)$. In the off state, *T(E)=0* for $E > E_V$ and 1 for $E < E_V$ (ignoring scattering). We can simply set T(E) = 1, because the limits of integration are for $E < E_V$. The density of modes is given by$M(E) = W(g_V/\pi\hbar)\sqrt{2m_h^*(E_V - E)}$, where g_v is the Valley degeneracy (which is 2 for the case of Tellurene), W is the width of sample and m_h^* is the hole effective mass in valance band (m_h^* for Tellurene is 0.26 m_0)[175].

Overall we can write as,

$$I = V_{ds}W\frac{2q^2}{h}\frac{g_V}{\pi\hbar}\frac{\sqrt{2m_h^*}}{k_BT}\int_{-\infty}^{E_V}\sqrt{(E_V - E)}\, e^{\frac{-(E_{F0}-E)}{k_BT}}dE$$

By expressing the SB height as $\phi_{SB} = E_{F0} - E_V$ and writing $x = \sqrt{(E_V - E)}$ we obtain

$$I = V_{ds} W \frac{2q^2}{h} \frac{g_V}{\pi\hbar} \frac{\sqrt{2m_h^*}}{k_B T} e^{\frac{-\phi_{SB}}{k_B T}} 2 \int_0^\infty x^2 \, e^{-x^2/k_B T} dx$$

Finally, using $\int_0^\infty x^2 \, e^{-ax^2} dx = \frac{1}{4}\sqrt{\frac{\pi}{a^3}}$ we obtain

$$I = V_{ds} W K \sqrt{k_B T} e^{-\phi_{SB}/k_B T}$$

Where, $K = \frac{q^2}{h} \frac{g_V}{\hbar} \sqrt{\frac{2m_h^*}{\pi}}$

As depicted in **Figure 5.8a** through the band diagram, when the device is biased in the off-state, the barrier height (Φ_B) is established by the energy differential between the top of the valence band in the channel and the Fermi-level at the contact. At "flat-band," Φ_B corresponds to the Schottky Barrier (SB) height for holes (Φ_{SB}). The likelihood of holes occupying energy levels available for conduction in the valence band (i.e., above the barrier) experiences an exponential increase with rising temperature. Hence, thermionic current exhibits an exponential rise with temperature. The experimental determination of the barrier height involves analyzing the slope of the plot of $\log(I/V_{ds} W K \sqrt{k_B T})$against $1/T$ as shown in **Figure 5.8b**. The extracted Φ_{SB} as a function of V_{bg} are plotted in **Figure 5.8c**. Beyond the flat-band condition, the interface barrier remains constant. However, the extracted Φ_{SB} continues to decrease, albeit at a slower pace. This decline is attributed to the growing influence of thermally assisted tunneling. The flat-band state is identified by observing a deviation from the linear dependence of Φ_{SB} with respect to V_{bg}. The extracted Schottky barrier height in Device 1 is around 28 meV, which is much smaller than the previously reported 60 meV in platinum contacted device[178]. Such a small Schottky barrier height in the Tellurene FET is in consistent with the dominant p-type conduction in the device. The field effect mobility, calculated using the relation $\boldsymbol{\mu_{FE} = L/(WC_{ox}V_{ds})gm}$, is depicted as a function of temperature in **Figure 5.8d**. Notably, the mobility shows a near plateau-like behavior below approximately 220 K, indicating a saturation effect. However, as temperature rises, there is a pronounced decline in mobility. This decline at higher temperatures is likely attributed to the

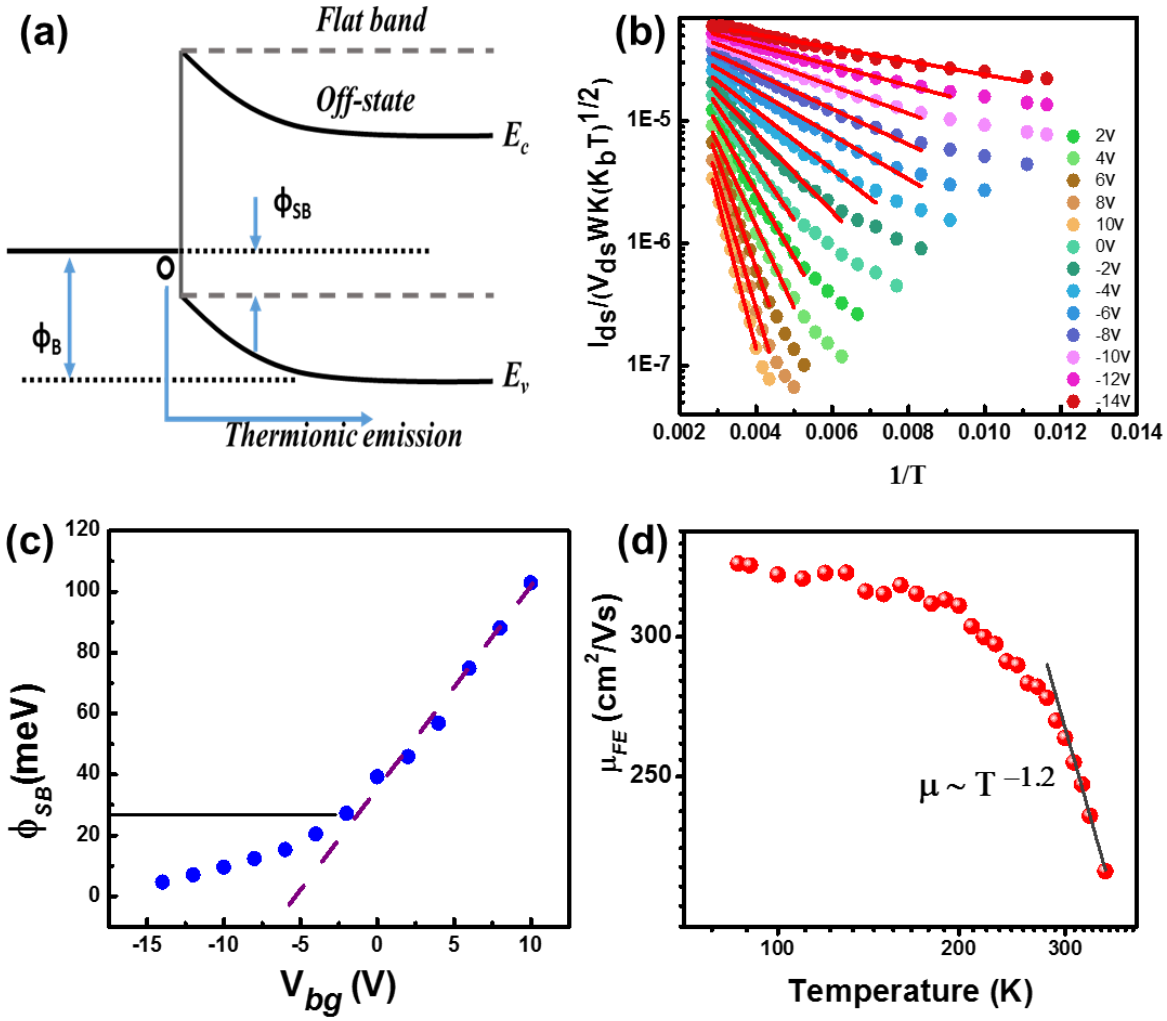


Figure 5.8. *(a) Band diagram shows barrier for holes. (b) Arrhenius-type plot of I_{off} vs 1/ T at different V_{bg} (c) Variation of the extracted barrier heights for device at different gate voltage. (d) Calculated field effect mobility is plotted at various temperature.*

increased phonon scattering, a phenomenon that can be accurately described by the expression $\mu \sim T^{-\gamma}$, with an exponent value of $\gamma = 1.2$. Acoustic phonon scattering is anticipated to yield $\gamma = 1$, whereas $\gamma > 1$ indicates that optical phonon scattering is the predominant mechanism for scattering. Values of γ near 1.2 imply that the mobility in our multilayer Tellurene device is predominantly influenced by optical phonon scattering. This finding aligns well with previously reported cases for MoS_2 transistors[6,13,163,194,196]. Furthermore, the observed saturation of mobility at low temperatures strongly suggests minimal influence from charge impurity scattering.

5.6 Low frequency noise in Tellurene FET

After characterizing the time-averaged transport behavior in these devices, we focused on the low frequency noise or current fluctuations at room temperature. The measurements are performed using ac lock-in amplifier-based technique as described in Chapter 2. We limited ourselves to the Ohmic regime to get the dominant contribution from the channel, rather than the interface barrier. First, we measure the noise at different current bias at V_{bg} = 0 V and observe that the noise PSD scales linearly with the square of the current, as expected from the Ohmic conductor (**Figure 5.9a**).

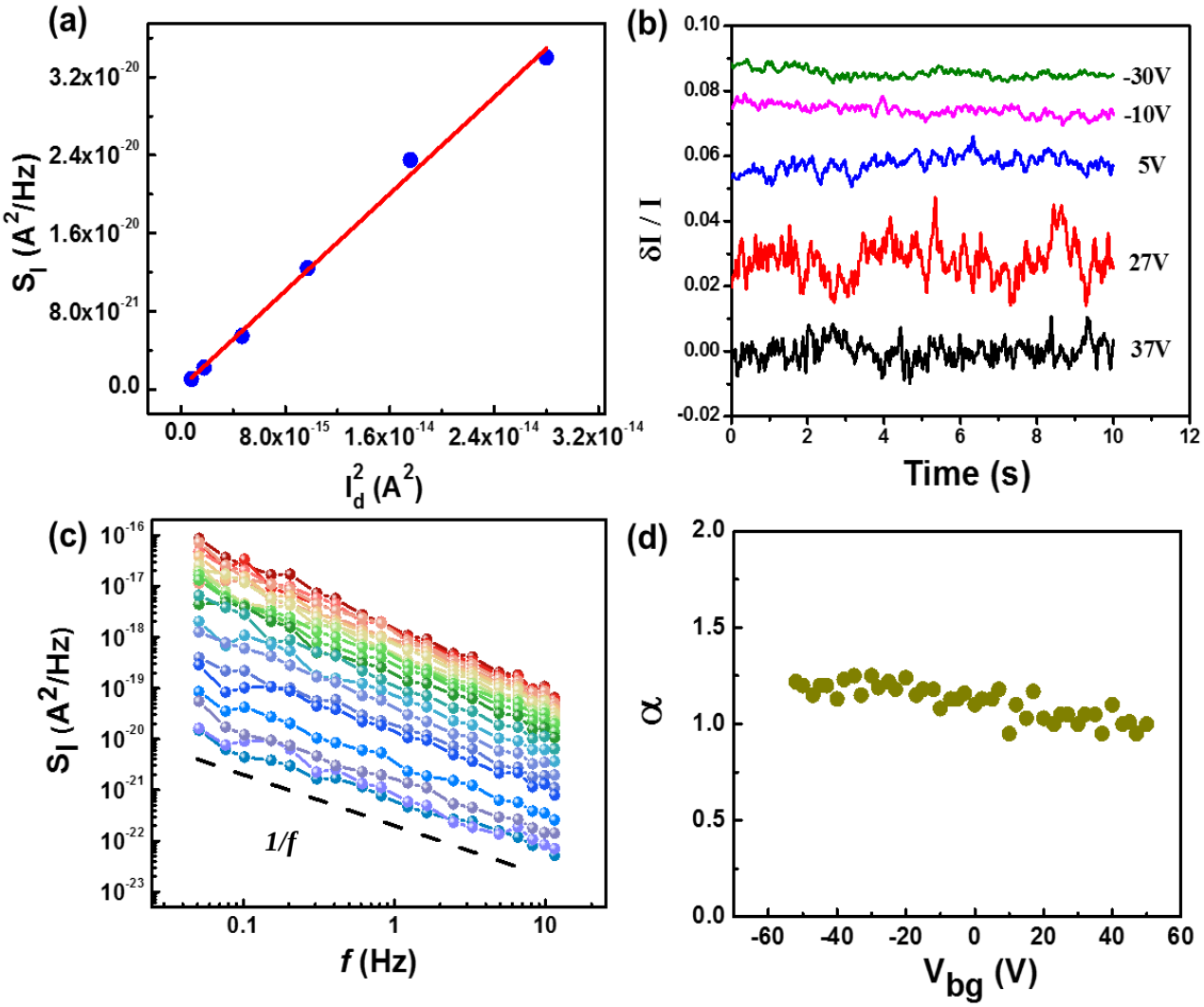


Figure 5.9. *(a) Variation of noise power spectral density, S_I with the square of the drain current, exhibiting linear behavior. (b) Time domain current fluctuation recorded at various gate-voltages as specified. (c) Noise power spectra S_I at various V_{bg}, showing 1/f characteristics. (d) shows that the variation of α with V_{bg} and it lies between 0.9-1.2.*

Subsequently, we measure the noise as a function of gate bias by choosing an ac bias of 100 mV at a carrier frequency of 222 Hz. The noise power spectra for different gate voltages as shown in **Figure 5.9c** follow mostly $1/f^{\alpha}$ behavior with α varies within the range, 0.9-1.2 (**Figure 5.9d**). To extract the amplitude of noise without enforcing any physical model, we have used the Hooge's empirical law derived for homogeneous conductor[83,197] :

$$\frac{S_I}{I^2} = \frac{A}{f^{\alpha}} = \frac{\alpha_H}{f^{\alpha} N}$$

Where S_I is the current power spectral density, I being the average source drain current. The noise PSD at f = 1 Hz is plotted with respect to the gate voltage, as shown in **Figure 5.10a**. We can see that the noise PSD decreases as we go in the larger -ve gate voltage and it increases significantly in the subthreshold region of the transfer characteristics. Electrical noise has been investigated in detail in field effect transistors fabricated by van der Waal materials like Graphene and other 2D semiconductors, and it is accepted that the charge fluctuations due to the interfacial traps closed to the channel are the dominant sources of low frequency noise[48,65,84,87,132,140,147,198,199] .The decrease in the noise figure at the ON state of the device is also observed in case of MoS_2, BP, $MoSe_2$ field effect devices[167,190,200,201], and it is attributed to the electrostatic screening effect by the high carrier density at the ON state of the device. In the subthreshold region where the ability to screen any background charge fluctuations reduces, resulting in a higher noise in that region. **Figure 5.10c** shows transfer characteristics and the corresponding gate dependent noise PSD (at 1 Hz) from another device (Device 3) having a higher thickness (approximately 60nm). As expected, the gating efficiency reduces due to the large thickness of the device and as a consequence it shows low I_{on}/I_{off} ratio. Concomitantly, the noise magnitude also decreases and follow similar gate dependence with decrease of noise with increasing hole carrier.

We next focus on the mechanism of noise in the present case. Previous studies on 2D FETs have explained that noise data can be explained using both carrier number fluctuation (CNF) model and the Hooge's mobility fluctuation (HMF) model (see Chapter 1. Section 1.5 for details about the noise models). In some cases, correlated number and mobility fluctuations model was considered instead of pure CNF model[84,85,202,203]. Slow trapping-detrapping of charge carriers by the interfacial traps results in the fluctuation in the change in the carrier number in the channel. The drain current noise spectral density due to the CNF model can be expressed as,

$$\frac{S_I}{I_{ds}^2} = S_{vfb}\left(\frac{g_m}{I_{ds}}\right)^2$$

where, g_m is the transconductance and S_{vfb} is the flat band voltage spectral density. In contrast to the CNF model, the HMF model assumes that the conductance noise originates as a result of the mobility fluctuation arising because of the fluctuations in the scattering process due to the number

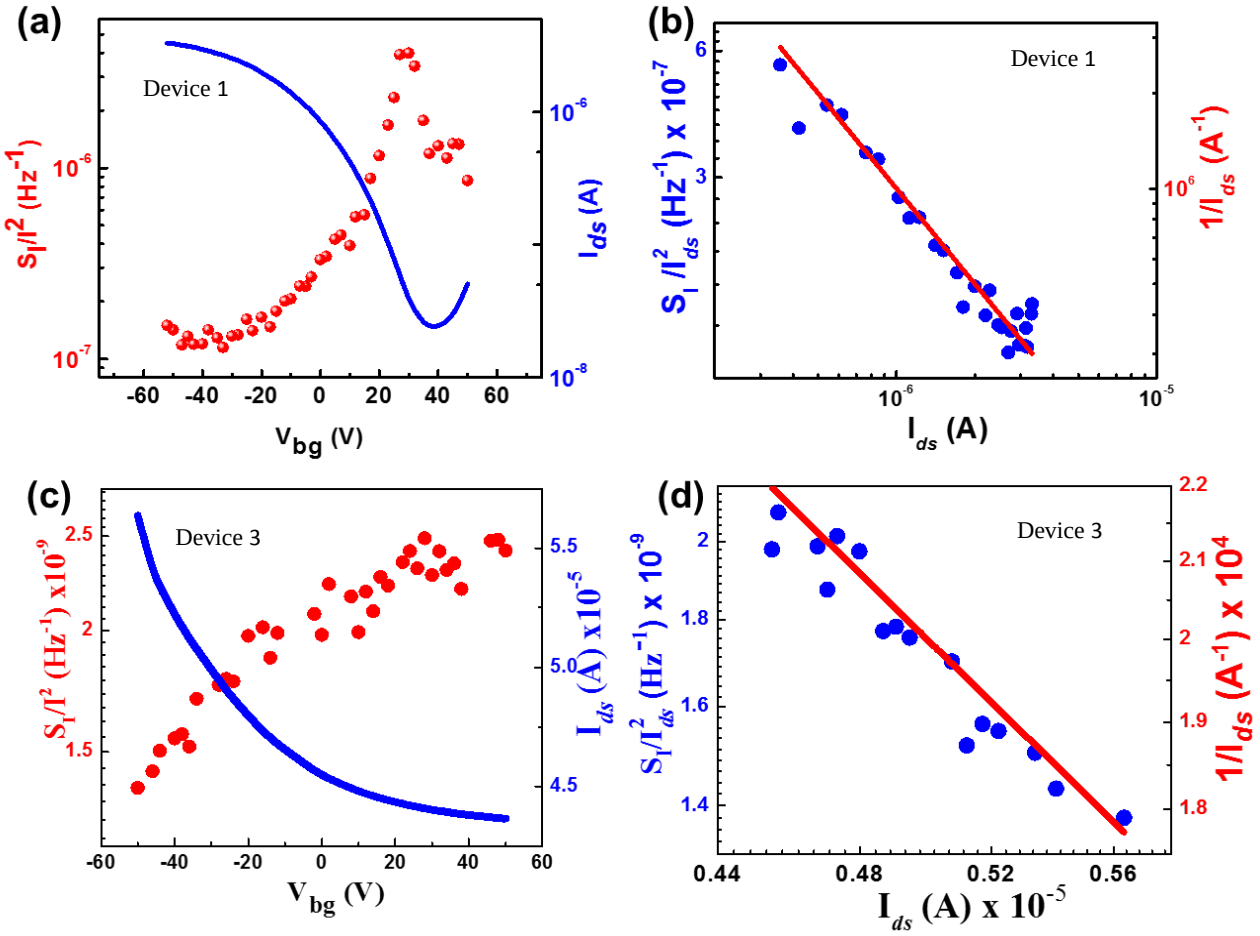


Figure 5.10. *(a) Variation of normalized noise PSD calculated at 1Hz (red data points) and the source drain current (blue line) with V_{bg}. A clear decrease in the noise at higher current is observed. (b) Variation of Noise PSD at 1 Hz (Blue dots) and the variation of $1/I_{ds}$ (red line) is plotted with I_{ds}, the calculated Noise PSD follow the trend of 1/Ids confirming the Hooge's mobility fluctuation model (c) Variation of normalized noise PSD (red data points) and the source drain current (blue line) with V_{bg} for a 60 nm thick Te FET.(d) Variation of Noise PSD (Blue dots) and the variation of $1/I_{ds}$ (red line) is plotted with I_{ds}, the calculated Noise PSD follow the trend of $1/I_{ds}$.(for 60 nm thick flake)*

fluctuation of phonon modes in the lattice. The drain current spectral density in case of HMF model is expressed as[86,204],

$$\frac{S_I}{I_{ds}^2} = \frac{q\alpha_H \mu_{eff} V_{ds}}{fL^2 I_{ds}},$$

where $\boldsymbol{\alpha_H}$ is the Hooge parameter, an empirical dimension-less constant, μ_{eff} is the effective mobility of the device.

To understand the mechanism of noise in our multilayer Tellurene device, we have plotted the S_I/I_d^2 as a function of I_d in log-log scale. For calculation we have only used the current above the threshold region of the p-branch of the device. The S_I/I_d^2 vs I_d and it follows the curve of 1/ I_d as shown in **Figure 5.10 b**, (for the case of bulk device the normalized PSD follows the $1/I_d$

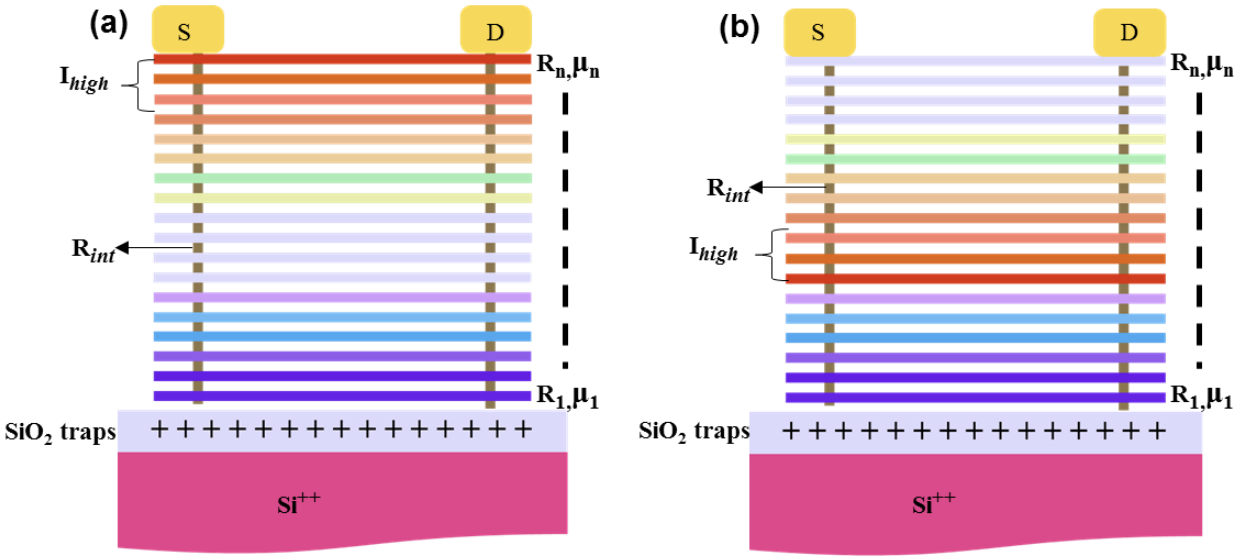


Figure 5.11. *Schematic model describing the flow of current in the different layers of the multilayer Tellurene device, at ON state (a) and in the OFF state (b).*

characteristics, as shown in the **Figure 5.10d**). This indicates that the flicker noise or the 1/*f* noise in our multilayer Tellurene device mainly originates from the Hooge's mobility fluctuation. This behavior of noise can be modeled using the resistive network model as proposed by Das. *et.al*. As suggested by the model, the comparatively high values of Thomas –Fermi screening length (λ), internal resistance (R_{int}) and the notable influence of charge impurity scattering, which significantly lowers the mobility of the bottom layers near the substrate. In a stack such as this one, the top layers are less resistive because their mobility values are higher, and a significant value of λ (4.8nm)[10] guarantees that a significant number of charges are filled in the top layers. Despite having a bigger charge population, the bottom layers are more resistant because of

their lower mobility values. At the same time, a high interlayer resistance value hinders the passage of current into the lower layers allowing current to pass mainly through the top layers (as indicated in red color (I_{high}) layer in **Figure 5.11 a**) close to the source drain contact. Most of the trapping detrapping of the charges occurs at the interface between the gate oxide and the channel, which gives rise to the CNF. Hence, for a multilayer Tellurene device, negligible current flows in the bottom layer (as indicated by the blue color layer in **Figure 5.11a**) resulting in a negligible CNF, most of the fluctuation in the current occurs directly from the phonon scattering from the top layer giving rise to mobility fluctuation in the entire region of FET operation. Hooge parameter ($\boldsymbol{\alpha_H}$), the most popular figure of merit, is extracted from the Hooge's empirical relationship

$$\frac{S_I}{I_d^2} = \frac{\alpha_H}{Nf}$$

Where, N is the total number of carriers in the channel and can be written as $N = (V_{GS} - V_{TH}) \times L \times W \times C_g/q$, where q is the elemental charge. By linear fitting the S_I/I^2 vs $1/(V_{GS} - V_{TH})$ curve we have extracted $\boldsymbol{\alpha_H}$ is about 1.34×10^{-2} which is in comparable to those of reported multilayer MoS_2 and hBN encapsulated $MoSe_2$ devices[8,30,201,205–211].

Table 2 . Comparison of Mobility and Hooge parameter reported in different samples.

Sample name	Thickness	Mobility (μ) (cm^2/Vs)	Hooge Parameter (α_H)	Reference
MoS_2	50 nm	20.27	0.01	[204]
MoS_2	Single layer	65	0.005	[200]
MoS_2	Single layer	18	0.15	[206]
WSe_2	27 nm	80	0.12	[30]
WSe_2	50 nm	60	0.007	[207]
$MoSe_2$	10 nm	100	0.002	[208]
$MoSe_2$	6.2 nm	10	0.708	[209]
ReS_2	7 nm	0.3	2×10^{-6}	[210]
BP	8.6 nm	47	0.014	[205]
BP	7.5 nm	90	2×10^{-4}	[8]
Te	20 nm	242	0.01	This work

5.7 Summary

- We've effectively produced 2D elemental semiconductor Tellurene through a hydrothermal approach. The resultant 2D Tellurene exhibits a crystalline structure, as validated by XRD and TEM examinations. The thickness of the flakes ranges from a few nanometers to tens of nanometers, with dimensions varying from 10 to 50 microns.

- The electrical transport measurement conducted on Tellurene flakes in its field-effect configuration indicates that it is predominantly a p-type semiconductor. The ambipolarity observed in the electrical transport measurement is sensitive to the sample's mobility. A sample of high quality, characterized by high mobility and good Ohmic contact, can exhibit both a high I_{on}/I_{off} ratio and ambipolar characteristics.

- From the temperature dependent transport of the Te FET we can conclude that the hysteresis in the transfer characteristics arising during the gate voltage sweep reduces at low temperatures. The observation indicates the reduction of active interfacial traps upon lowering temperature.

- In high mobility samples, we have noted a metal to insulator (MIT) transition occurring at elevated carrier densities. The temperature at which this transition takes place is contingent upon the carrier density within the system. Conversely, in low mobility Te FETs, this MIT transition is not observed even at high carrier densities.

- The Shottky barrier height represents a critical bottleneck for semiconductor field-effect transistors. Through an analysis of the temperature-dependent transfer characteristics of the Te FET, we have determined that the Schottky barrier height (Φ_{SB}) for the Cr/Au contacted Te FET is approximately 28 meV. This low Φ_{SB} in our Te FETs plays a pivotal role in promoting dominant p-type conduction in our devices. Additionally, the temperature-dependent mobility study unveils a robust electron-phonon scattering mechanism at higher temperatures (greater than 200 K). Conversely, the saturation of mobility at lower temperatures indicates minimal influence from charge impurity scattering.

- We have also performed the low frequency noise measurement in room temperature in the Te FET. Typical 1/f noise type of behavior is observed over entire range of gate voltages. The normalized PSD shows a peak in the off state because of the less screening effect due to smaller charge carrier densities. The normalized PSD above the subthreshold region the PSD follows $1/I_{ds}$ curve indicating that the noise is arising primarily due to mobility fluctuations.

Chapter 6

Conclusion

During the doctoral program, we focused on addressing fundamental inquiries concerning electronic transport in 2D materials and their hybrids. Our investigations have utilized temperature dependent transport studies based on conductance fluctuations, providing more intricate insights compared to standard transport measurements. Considering practical applications, these fluctuations in conductivity present a substantial bottleneck, hence a clear understanding of the origin of these fluctuations are essential. The performance of a Graphene device can be hindered by interface traps, Coulomb impurities, grain boundaries, or interfacial phonons. Many of these effects are originating from the substrate, emphasizing the crucial need to comprehend the substrate's impact on the transport properties of 2D materials. The primary source of resistance fluctuations in the Graphene channel is the trapping and de-trapping processes near the Graphene/substrate interface. Meanwhile, Coulomb fluctuations arising from charge fluctuations deep within the substrate bulk are effectively screened by the heavily doped substrate. Chapter 3 details the electrical transport and low-frequency noise properties of a large-area CVD Graphene field-effect transistor (FET) constructed on a lightly doped Si/ SiO_2 substrate ($N_A \sim 10^{15}$ cm^{-3}). This analysis involves a systematic examination of electrical transport, noise spectroscopy, and capacitance. These measurements are conducted across a range of voltages and temperatures to capture the device's response under diverse operating conditions. The key findings of the study reveal the presence of a resistance vs. gate voltage hump at room temperature. This phenomenon is attributed to a decrease in gate capacitance resulting from the formation of a depletion region at the SiO_2/Si interface. The impact is particularly notable in low-frequency noise, especially near V_{bg} = 0V. Temperature-dependent noise measurements, as well as capacitance and resistance assessments down to 77 K, establish a direct correlation between the observed noise and the formation of the depletion region. The proposed mechanisms for the noise involve fluctuations in bulk charge within the depletion region and the modulation of the energy level of interface traps. These factors contribute to mobility fluctuations in the Graphene channel. Further measurements on a top-gated device reveal behavior explainable by charge exchange processes between Graphene and interfacial traps near the surface. The overall conclusion emphasizes the sensitivity

of Graphene field-effect transistors to remote bulk charge fluctuations in lightly doped substrates. This findings are crucial not only for the integration of Graphene with existing silicon technology but also for providing fundamental insights into the impact of remote interfaces on electron transport in Graphene.

In chapter 4, we tried to functionalize Graphene-based materials (CVD Graphene and rGO) for the creation of a tunable memory device. Our approach involved employing an electrically insulating SCO (spin crossover) molecule, capable of transitioning from low spin to high spin under stimuli such as temperature, light, or pressure. Devices were constructed by grafting these SCO molecules onto both CVD Graphene and reduced Graphene oxide (rGO). Electrical transport measurements revealed a direct correlation with spin crossover in both cases as a function of temperature. In the CVD Graphene-SCO hybrid device, hysteresis could be tuned by controlling the gate voltage. In contrast, the rGO/SCO hybrid system allowed control of hysteresis width and transition temperature by varying molecular concentration. Magnetic measurement in rGO/SCO heterostructure further reveal that the interfacial charge transfer-induced intermolecular interaction in the heterostructure leads to improved cooperativity. The presence of both ferromagnetic (for the low coverage case) and anti-ferromagnetic (dominant for the high coverage sample) intra-chain interactions is established in the hybrid by the enhanced magnetic coupling of the heterostructure, which results in spontaneous magnetization states with a large coercive field.

With a goal to achieve a high mobility field effect transistor working at ambient condition and to overcome the problem of zero bandgap in Graphene, in Chapter 5, we have examined the trasnport and low frequency noise in a low bandgap semiconductor, Tellurene. Electrical transport measurements on Tellurene flakes in a field-effect configuration reveal its predominant p-type semiconducting nature. Ambipolarity observed in transport is correlated with sample mobility. High mobility samples exhibit a Metal to Insulator Transition (MIT) at elevated carrier densities, with the transition temperature dependent on carrier density. Conversely, low mobility Te FETs do not display the MIT transition even at high carrier densities. Analyzing temperature-dependent transfer characteristics, we determined the Φ_{SB} for Cr/Au contacted Te-FET to be approximately 28 meV. This low Φ_{SB} plays a pivotal role in promoting dominant p-type conduction. Additionally, the temperature-dependent mobility study reveals a robust electron-phonon scattering mechanism at higher temperatures (> 200K), while saturation of mobility at lower temperatures suggests

minimal influence from charge impurity scattering. Low-frequency noise measurements at room temperature in the Te FET exhibit typical 1/f behavior over the entire gate voltage range. The normalized Power Spectral Density (PSD) shows a peak in the off state due to reduced screening effects from smaller charge carrier densities. Above the subthreshold region, the normalized PSD follows a 1/Ids curve, indicating mobility fluctuations.

Future scope of study

In this thesis, some experimental setups were developed, and electrical transport and noise measurement were carried out to understand the effect of disorder determining the transport and to prepare some functional devices out of it. Although there are many aspects which remain unaddressed in this work and can be extended for future work.

- It has been observed the substrate plays an important role in the quality of the device, because the trapped charges in the interface between the Graphene and dielectric plays a crucial role in the scattering mechanism. One could look into quantifying the trapped charges by the systematic measurement of the electronic transport and capacitance measurement such as deep level transient spectroscopy (DLTS) in different substartes.

- The significance of electrical contact lies in their role in determining the Schottky barrier height. It is crucial to identify device structures for Tellurene in which the barrier height is minimized. This necessitates an exploration of contact engineering within this specific device structure for future applications.

- The manipulation of the band structure of 2D materials has been demonstrated through the application of a perpendicular electric field. In particular, Tellurene exhibits characteristics of a Weyl semiconductor. It is worth investigating the transport behavior in presence of high electric fields generated in a dual gated structure and high magnetic field at low temperatures that may unravel possible emergent phases.

- We have shown that Graphene can be functionalized by adorning it with spin crossover molecules (SCO). This new composite material has opened a new possibility to create a controlled device for possible memory application. Achieving tunability of spin crossover

mechanism is certainly new and designing the material with transition temperature close to room temperature is possible and hence, demands more systematic investigation. Further insights into the mechanism of sensing spin switching can be gained by investigating noise measurements in high-quality devices with minimal base noise. Preferably, such studies should be conducted in a graphite-gated hexagonal boron nitride (hBN) encapsulated Graphene.

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